# Chapter 10 Integer-N Frequency Synthesizers

- 10.1 General Considerations
- 10.2 Basic Integer-N Synthesizers
- 10.3 Settling Behavior
- 10.4 Spur Reduction Techniques
- 10.5 PLL-Based Modulation
- 10.6 Divider Design
- 13.4 Synthesizer Design
- Simulations of PLL Transfer Function

# Chapter Outline

**Basic Synthesizer**

- ✓ Settling Behavior
- ✓ Spur Reduction Techniques

**PLL-Based Modulation**

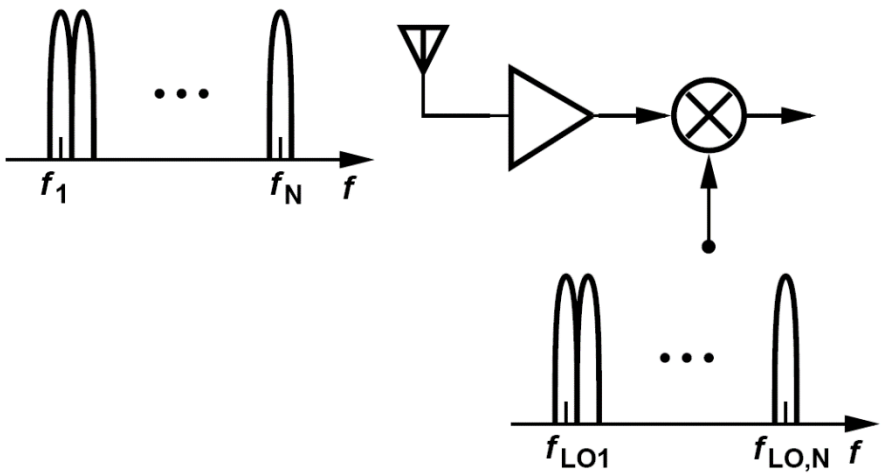
- ✓ In-Loop Modulation
- ✓ Offset-PLL TX

**Divider Design**

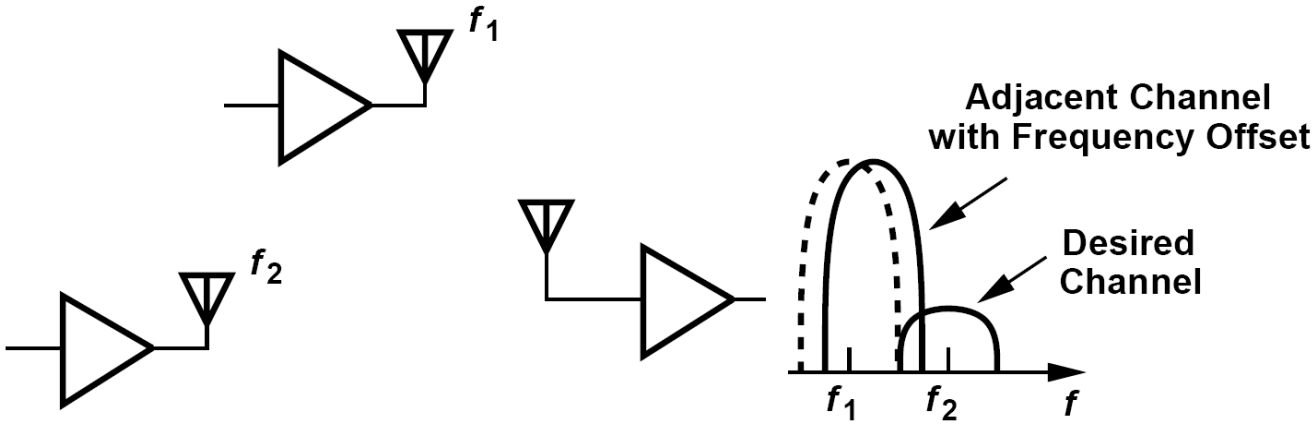
- ✓ Pulse-Swallow Divider
- ✓ Dual-Modulus Dividers
- ✓ CML and TSPC Techniques
- ✓ Miller and Injection-Locked Dividers

- ➢ Synthesizer Design
- ➢ Simulations of PLL Transfer Function

# General Considerations: Why We Need Synthesizers?

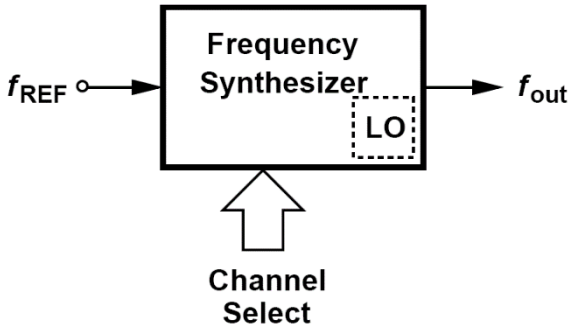



- The synthesizer performs the precise setting of LO frequency

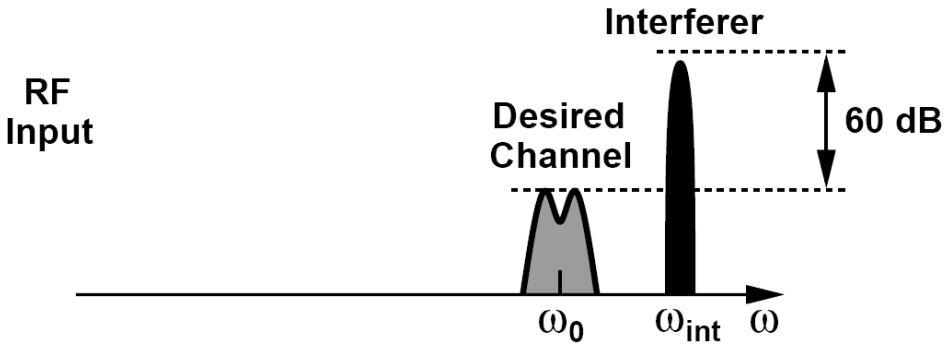


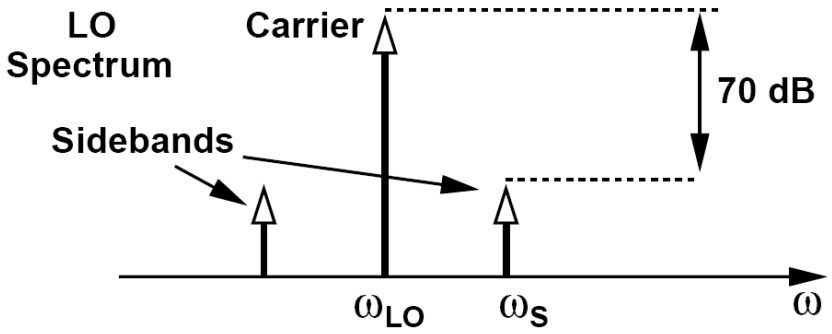

- A slight shift leads to significant spillage of a high-power interferer in to a desired channel

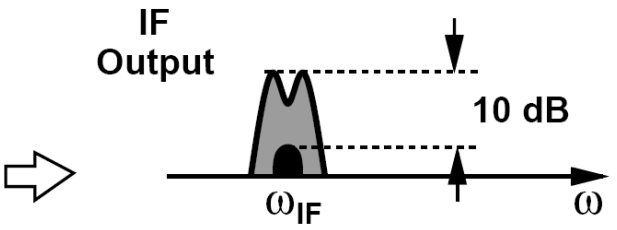
# Reciprocal Mixing




- The output frequency is generated as a multiple of a precise reference.
- Sidebands: upon downconversion mixing, the desired channel is convolved with the carrier and the interferer with the sideband

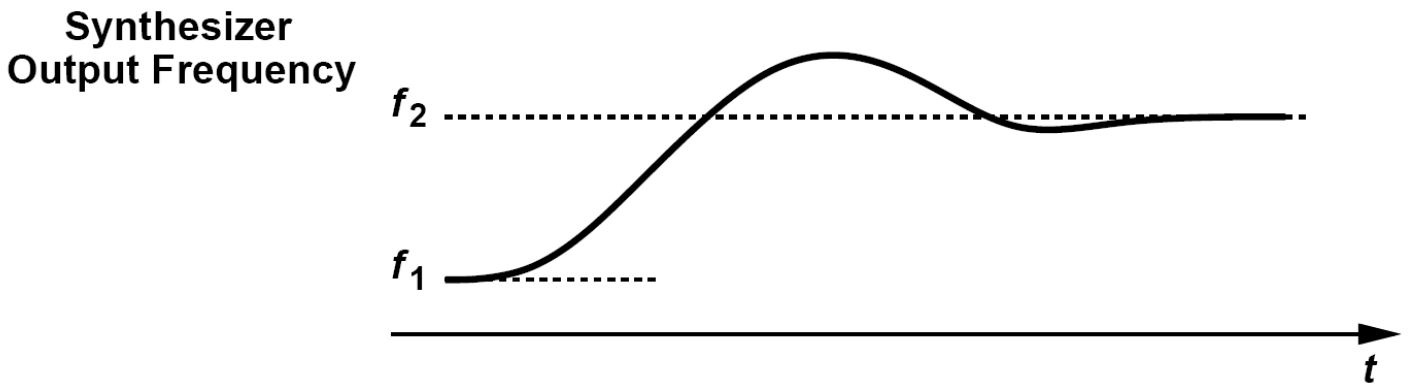


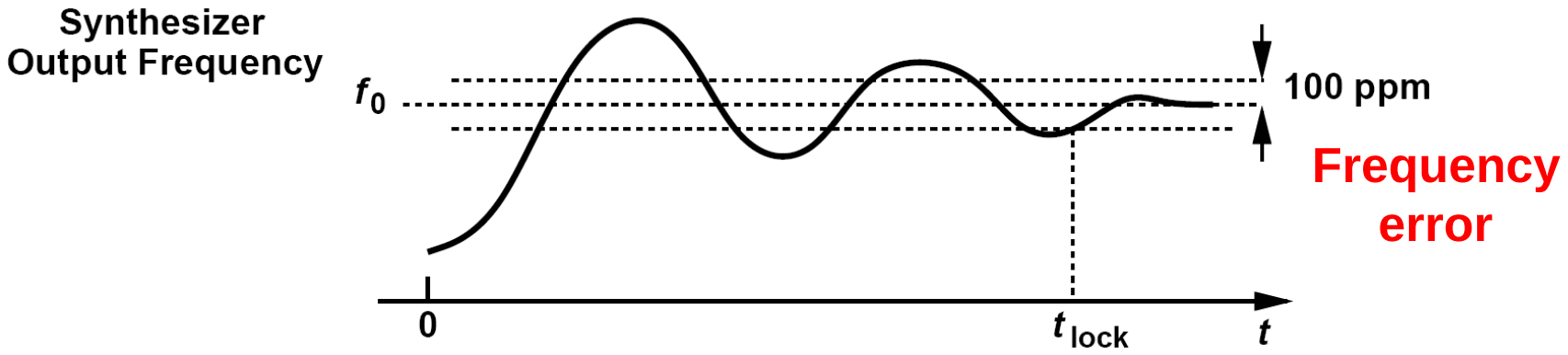




$$\omega_o - \omega_{LO} = \omega_{int} - \omega_s \equiv \omega_{IF}$$

# Lock Time

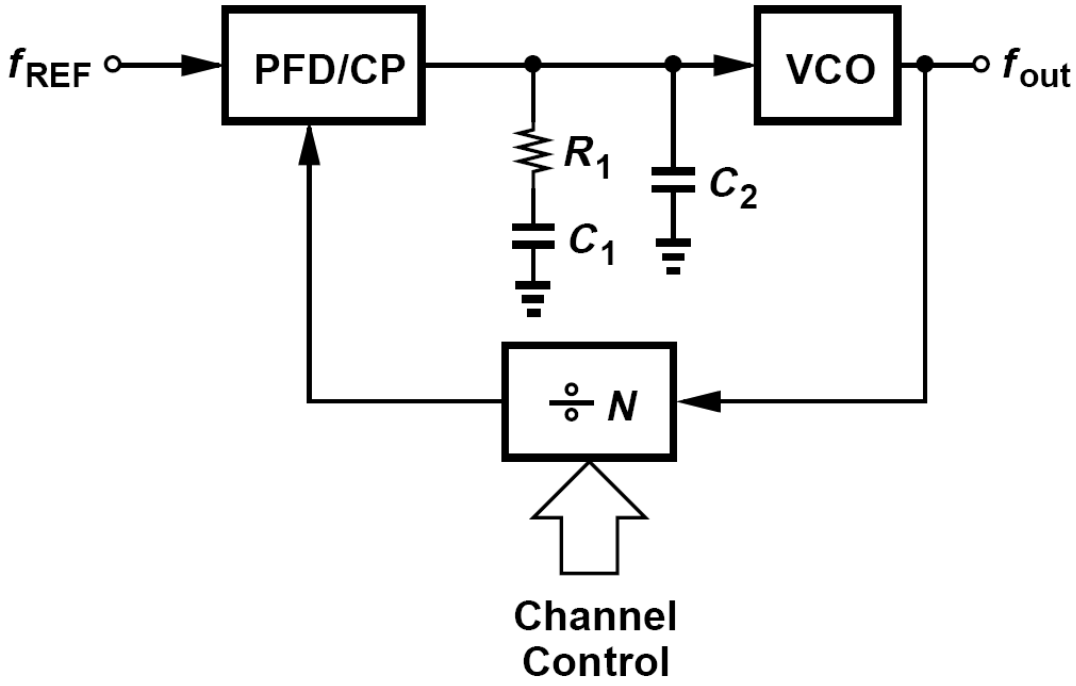



- **Lock time directly subtracts from the time available for communication**



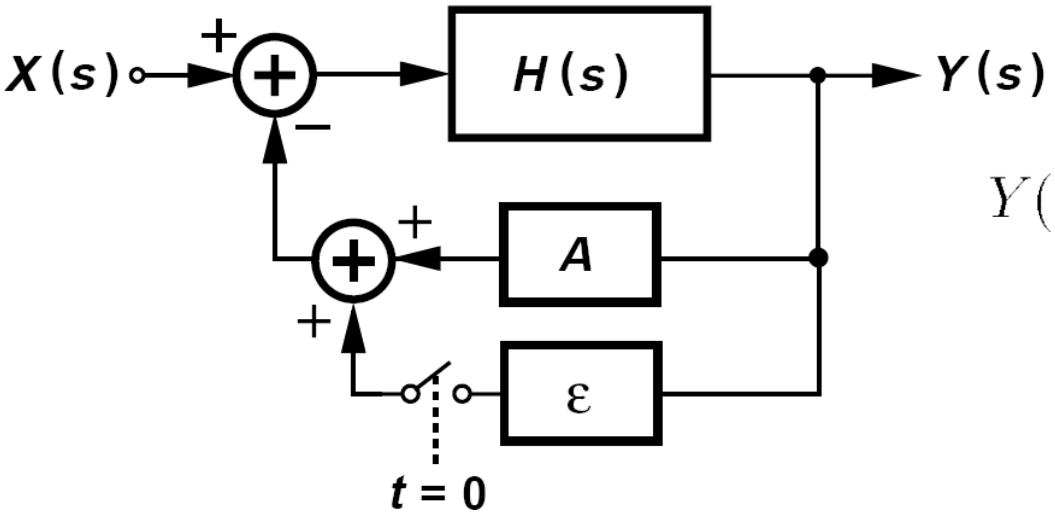

- **The lock time is typically specified as the time required for the output frequency to reach within a certain margin around its final value**

# Basic Integer-N Synthesizer




- Integer-*N* synthesizer produce an output frequency that is an integer multiple of the reference frequency.
- The choice of $f_{REF}$: it must be equal to the desired channel spacing and it must be the greatest common divisor of $f_1$ and $f_2$.

# Settling Behavior: Channel Switching

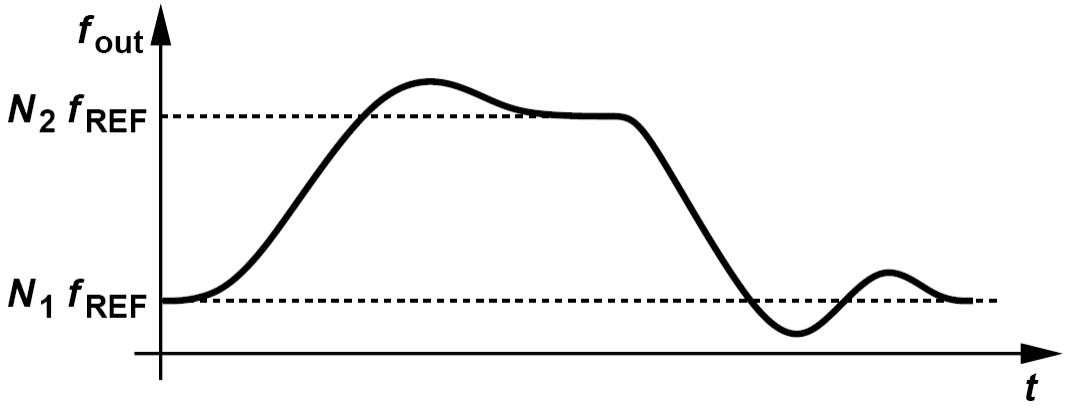



$$
\begin{aligned}
Y(s) &= \frac{H(s)}{1+(A+\epsilon)H(s)}X(s) \\
&\approx \frac{H(s)}{1+AH(s)} \cdot \frac{1}{1+\epsilon/A}X(s) \\
&\approx \frac{H(s)}{1+AH(s)}\left(1-\frac{\epsilon}{A}\right)X(s)
\end{aligned}
$$

**Retaining the transfer function, an equivalnet multiplication by (1 –$\varepsilon/A$) as a step function from $f_0$ to $f_0(1 - \varepsilon/A)$, i.e., a frequency jump of $-(\varepsilon/A)f_0$.**

- **When the divide ratio changes, the loop responds as if an input frequency step was applied**

# Worst Case Settling and Example of Error




- **The worse case occurs when the synthesizer output frequency must go from the first channel, $N_1 f_{REF}$, to the last, $N_2 f_{REF}$, or vice versa**

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**In synthesizer settling, the quantity of interest is the frequency error, $\Delta\omega_{out}$, with respect to the final value. Determine the transfer function from the input frequency to this error.**

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**The error is equal to $\omega_{in}[N - H(s)]$, where $H(s)$ is the transfer function of a type-II PLL (Chapter 9). Thus,**

$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{\omega_{out}}{\omega_{in}}(s) = H(s) = N\frac{2s\zeta\omega_n + \omega_n^2}{s^2 + 2s\zeta\omega_n + \omega_n^2}$$

$$\frac{\Delta\omega_{out}}{\omega_{in}} = N\frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

# Calculation of Settling Time

**Assuming N2-N1<<N1. If the divide ratio jumps from N1 to N2, this change is equivalent to an input frequency step of $\Delta\omega_{in}=(N2-N1)\omega_{REF}/N1$. The settling time should be normalized by the output frequency $N_2\omega_{REF}$. The normalized error to fall below a certain amount, α, will be**

$$\left|\frac{\omega_{ref}(N_2-N_1)-\Delta\omega_{out}}{\omega_{out,final}}\right| \equiv \left|\frac{\omega_{ref}(N_2-N_1)-\frac{(N_2-N_1)\omega_{ref}}{N_1}H(s)}{N_2\omega_{ref}}\right| \le \alpha \quad , H(s)=N_1\frac{2s\zeta\omega_n+\omega_n^2}{s^2+2s\zeta\omega_n+\omega_n^2}$$

$$\Rightarrow \left|1-\frac{N_1}{N_2}\right|\cdot\left|1-\frac{H(s)}{N_1}\right| \le \alpha$$

$$\left|1-\frac{N_1}{N_2}\right| g(t)u(t) \le \alpha \, , g(t)=e^{-\zeta\omega_n t}\left[\cos\left(\omega_n\sqrt{1-\zeta^2}\cdot t\right)-\frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(\omega_n\sqrt{1-\zeta^2}\cdot t\right)\right], \zeta<1 \quad (10.8)$$

**For example, if ζ= $\sqrt{2}/2$,**

$$\left|1-\frac{N_1}{N_2}\right|\left(\cos\frac{\omega_n t_s}{\sqrt{2}}-\sin\frac{\omega_n t_s}{\sqrt{2}}\right)e^{-\omega_n t_s/\sqrt{2}}=\alpha$$

$$\left|1-\frac{N_1}{N_2}\right|\sqrt{2}e^{-\omega_n t_s/\sqrt{2}}=\alpha \Rightarrow t_s=\frac{\sqrt{2}}{\omega_n}\ln\left|\sqrt{2}\left(1-\frac{N_1}{N_2}\right)\frac{1}{\alpha}\right|$$

# Example : Settling Time Calculation

**A 900-MHz GSM synthesizer operates with $f_{REF}$ = 200 kHz and provides 128 channels. If ζ= $\sqrt{2}/2$, determine the settling time required for a frequency error of 10 ppm.**

**The divide ratio is approximately equal to 4500 and varies by 128, i.e., $N_1 \approx 4500$ and $N_2 - N_1 = 128$. Thus,**

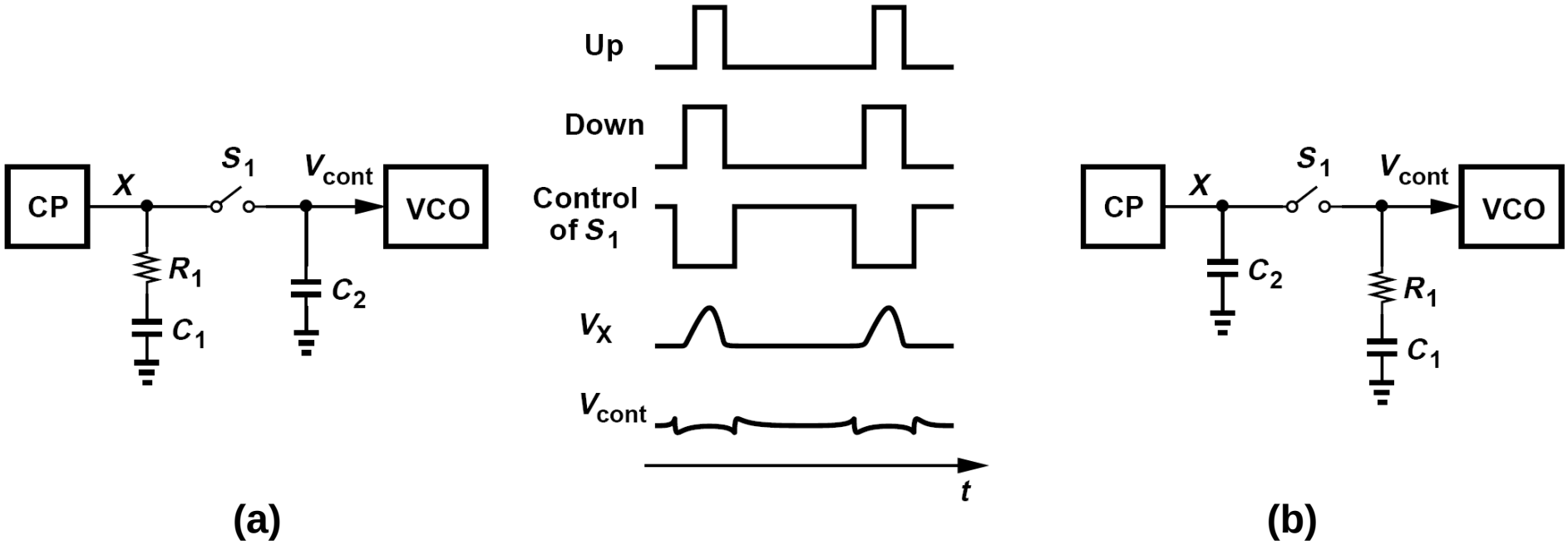
$$t_s \approx \sqrt{2}\frac{8.3}{\omega_n} \quad \text{or} \quad t_s = \frac{8.3}{\zeta\omega_n}$$

**From Chapter 9, we note that the loop time constant is roughly equal to one-tenth of the input period. It follows that $(\zeta\omega_n)^{-1} \approx 10T_{REF}$ and hence**

$$t_s \approx 83T_{REF}$$

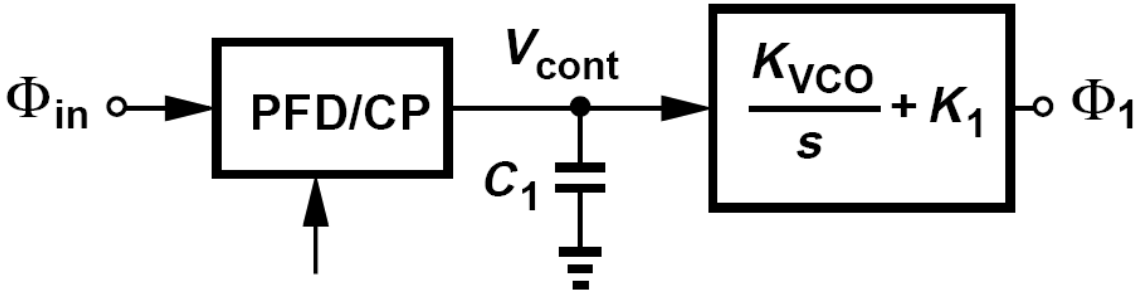
**In practice, the settling time is longer and a rule of thumb for the settling of PLLs is 100 times the reference period.**

# Spur Reduction Techniques: Masking the Ripple by Insertion of a Switch




- $V_{cont}$ is disturbed for a short duration (at the phase comparison instant) and remains relatively constant for the rest of the input period.
- The arrangement of (a) leads to an unstable PLL. (∵ As Vx was settled, Vcont senses the voltage is independent of R1. R1 has no function to serve as a zero)
- Topology of (b) can yield a stable PLL.

# Spur Reduction Techniques: Stabilization of PLL by Adding $K_1$ to the Transfer Function of VCO (I)




**Open-loop transfer function of a type-II second-order PLL**

$$H_{open}(s) = \frac{I_P}{2\pi}\left(R_1 + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{s}$$

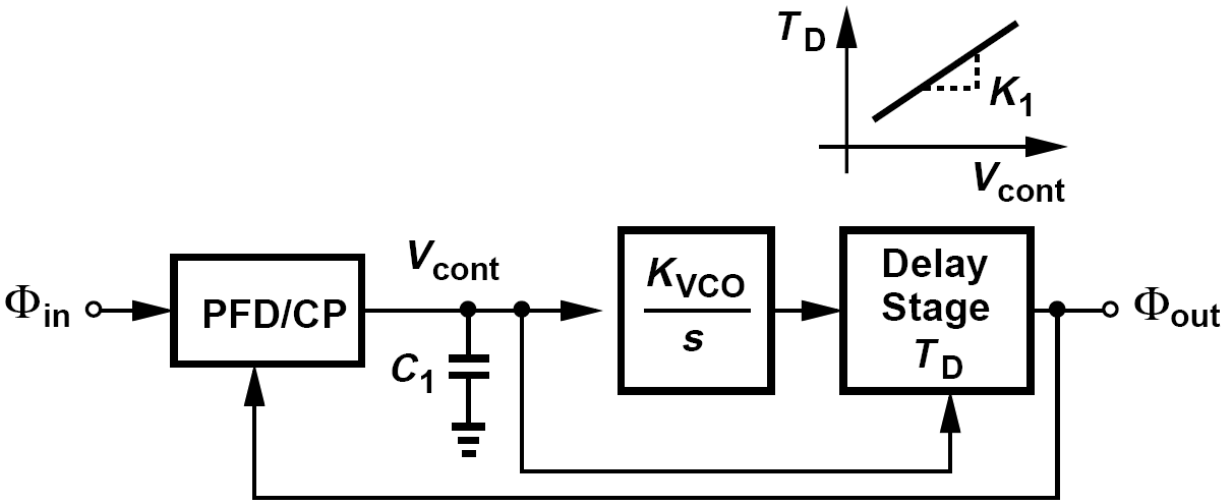
**Can we realize:** $$H_{open}(s) = \frac{I_P}{2\pi}\frac{1}{C_1 s}\left(\frac{K_{VCO}}{s} + K_1\right)$$ **to obtain a zero?**

$$\frac{\phi_1}{V_{cont}}(s) = \frac{K_{VCO}}{s} + K_1$$

**Indeed, $K_1$ represents a variable-delay stage having a "gain" of $K_1$:**

$$K_1 = \frac{\Delta T_d}{\Delta V_{cont}}$$

# Stabilization of PLL by Adding $K_1$ to the Transfer Function of VCO (II)

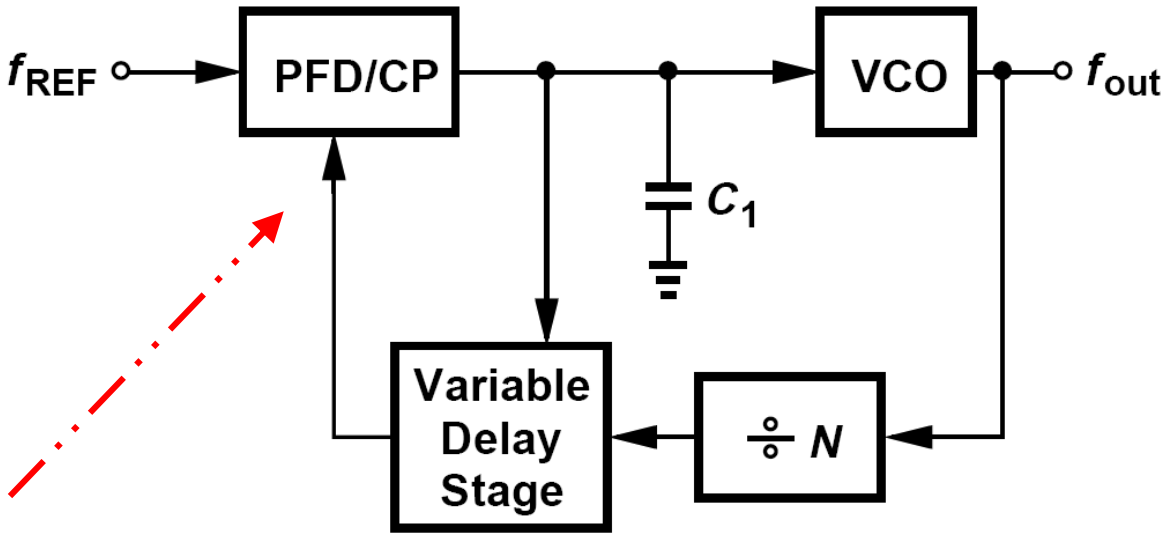



$$H_{closed}(s) = \frac{\frac{I_P}{2\pi C_1 s}(\frac{K_{VCO}}{s}+K_1)}{1+\frac{I_P}{2\pi C_1 s}(\frac{K_{VCO}}{s}+K_1)} = \frac{\frac{I_P K_1}{2\pi C_1}s+\frac{I_P K_{VCO}}{2\pi C_1}}{s^2+\frac{I_P K_1}{2\pi C_1}s+\frac{I_P K_{VCO}}{2\pi C_1}}.$$

$$\zeta = \frac{K_1}{2}\sqrt{\frac{I_P}{2\pi C_1 K_{VCO}}}$$

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1}}$$

# Stabilization of PLL by Adding $K_1$ to the Transfer Function of VCO: Modified Architecture

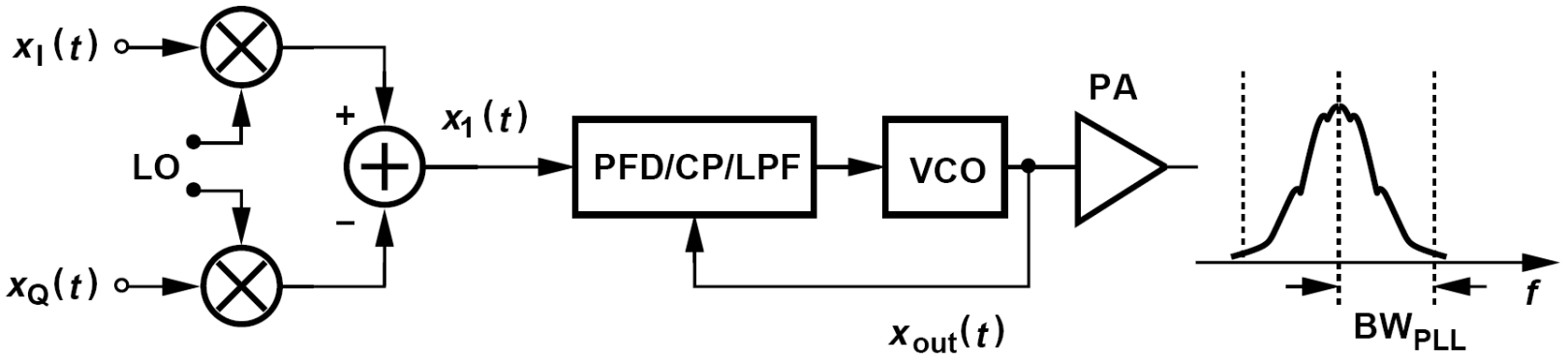



$$\zeta = \frac{K_1}{2}\sqrt{\frac{I_P N}{2\pi C_1 K_{VCO}}} \qquad \omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1 N}}.$$

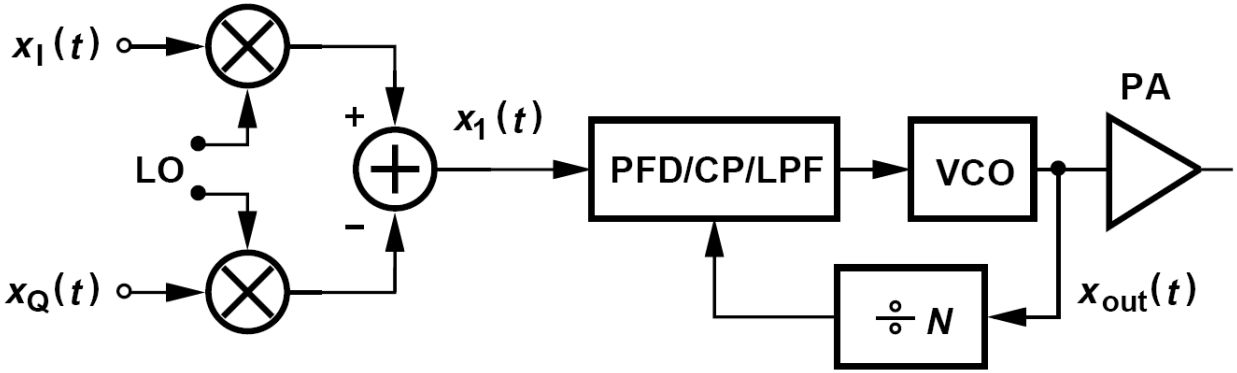
- **A retiming flip-flop can be inserted between the delay line and the PFD to remove the phase noise of the former**

IEEE JSSC, pp. 626-, Mar. 2016
IEEE JSSC, pp. 2117-, Aug. 2017

# Noise Filtration by Means of a PLL



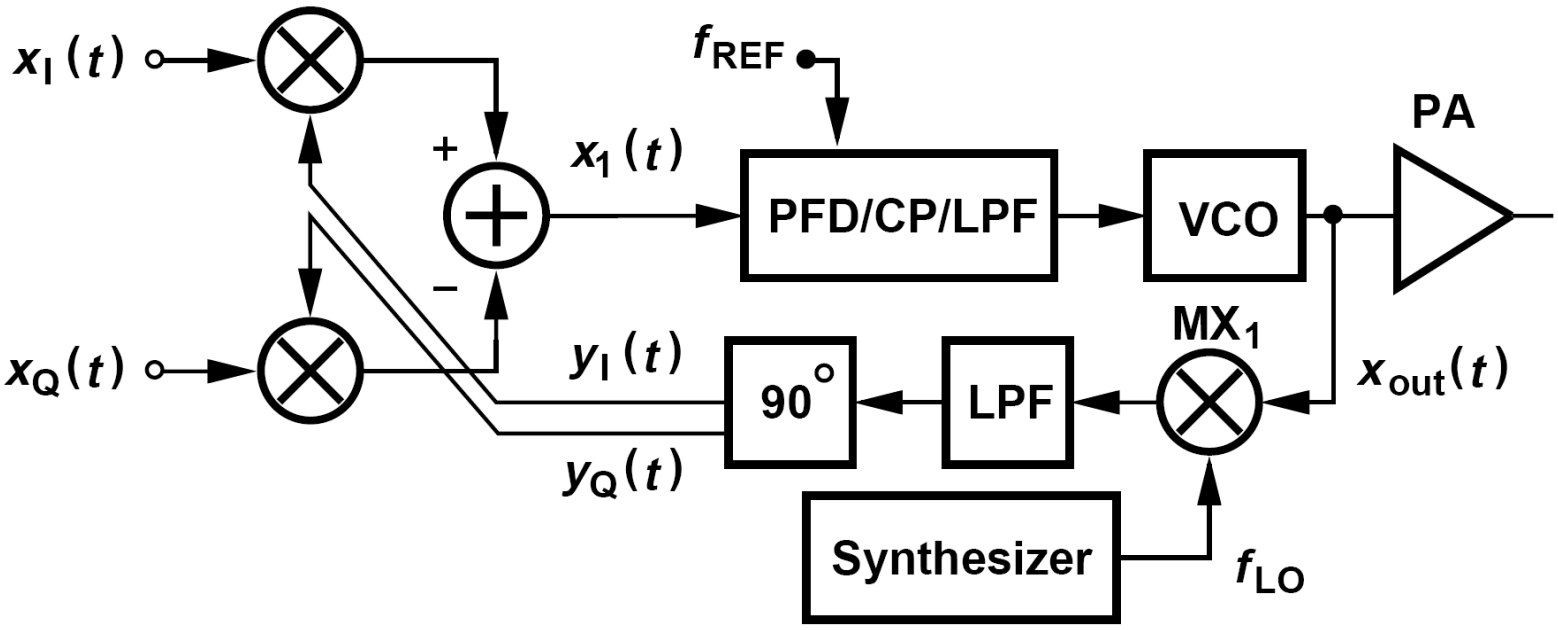

- $x_I(t)$ and $x_Q(t)$ : quadrature baseband signals; LO: $A\cos(\omega_1 t)$ and $A\sin(\omega_1 t)$ ; $x_1(t)=A\cos(\omega_1 t+\varphi(t))$ ; $x_{out}(t)=B\cos(N\omega_1 t+N\varphi(t))$




$$x_1(t) = A_1 \cos[\omega_1 t + \phi(t)] \quad \Rightarrow \quad x_{out}(t) = A_2 \cos[N\omega_1 t + N\phi(t)]$$

- The PLL multiplies the phase by a factor of *N*, altering the signal bandwidth and modulation

# Offset-PLL Architecture




- With the loop locked, $x_1(t)$ must become a faithful replica of the reference input, thus containing no modulation. Consequently, $y_I(t)$ and $y_Q(t)$ "absorb" the modulation information of the baseband signal.

# Example : Offset-PLL Architecture

If $x_I(t) = A\cos[\Phi(t)]$ and $x_Q(t) = A\sin[\Phi(t)]$,

Centered around $f_{REF}$, $y_I$ and $y_Q$ can be respectively expressed as

$$y_I(t) = a\cos[\omega_{REF}t + \phi_y(t)]$$
$$y_Q(t) = a\sin[\omega_{REF}t + \phi_y(t)],$$

where $\omega_{REF} = 2\pi f_{REF}$ and $\Phi_y(t)$ denotes the phase modulation information. Carrying the quadrature upconversion operation and equating the result to an unmodulated tone, $x_1(t) = A\cos\omega_{REF}\,t$, we have

$$A_1 a\cos[\phi(t)]\cos[\omega_{REF}t + \phi_y(t)] - A_1 a\sin[\phi(t)]\sin[\omega_{REF}t + \phi_y(t)] = A\cos\omega_{REF}t.$$

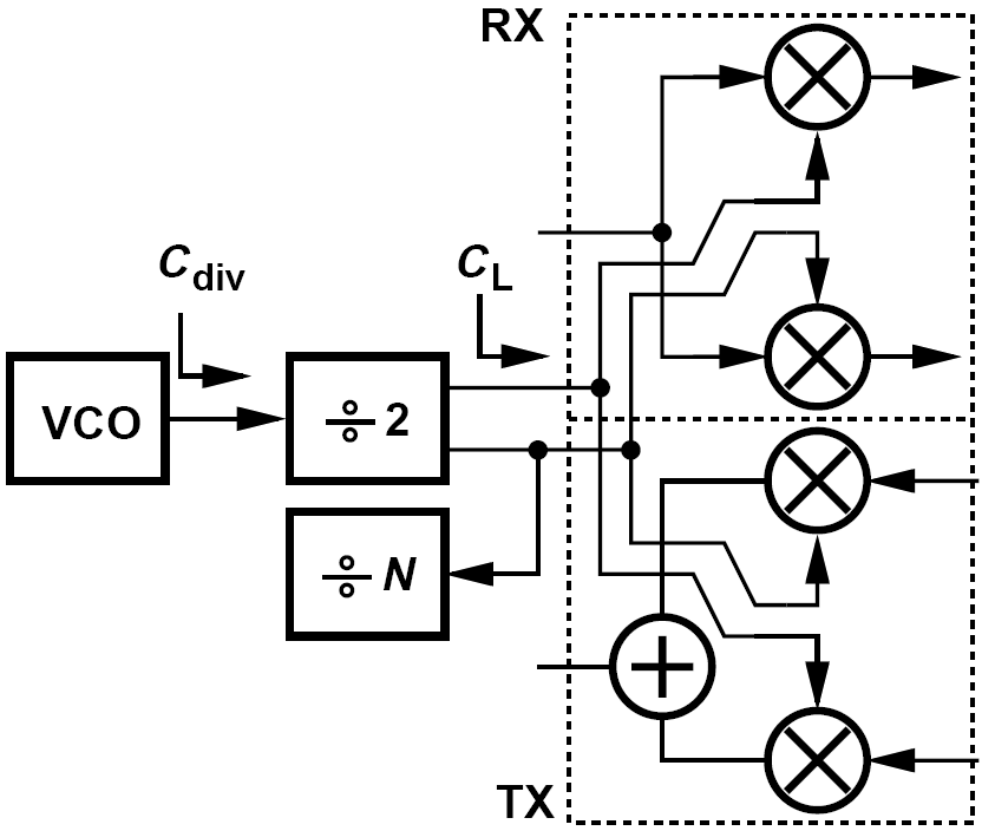
It follows that $A_1 a\cos[\omega_{REF}t + \phi(t) + \phi_y(t)] = A\cos\omega_{REF}t$

And hence $\phi_y(t) = -\phi(t)$

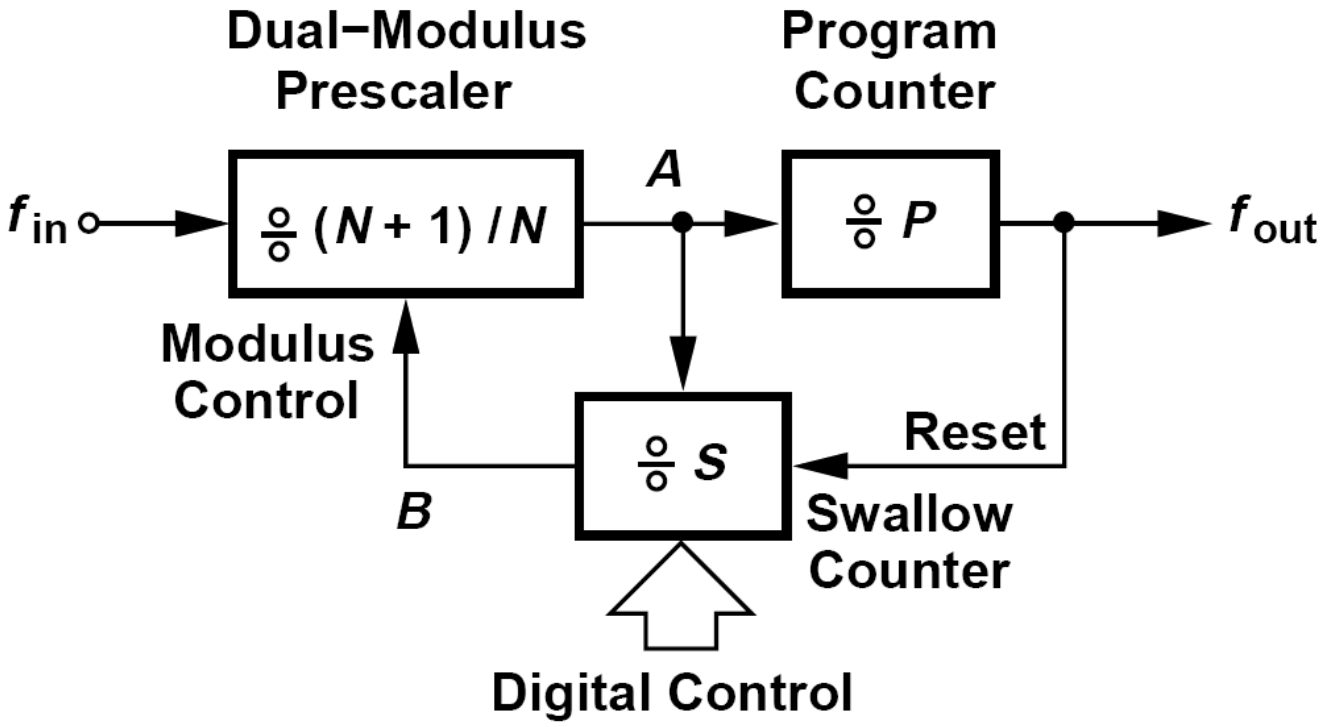
Note that $x_{out}(t)$ also contains the same phase information $\Phi_y(t)$.

# Divider Design: Requirements

- The divider modulus, *N*, must change in unity steps
- The first stage of the divider must operate as fast as the VCO
- The divider input capacitance and required input swing must be commensurate with the VCO drive capability
- The divider must consume low power, preferably less than the VCO

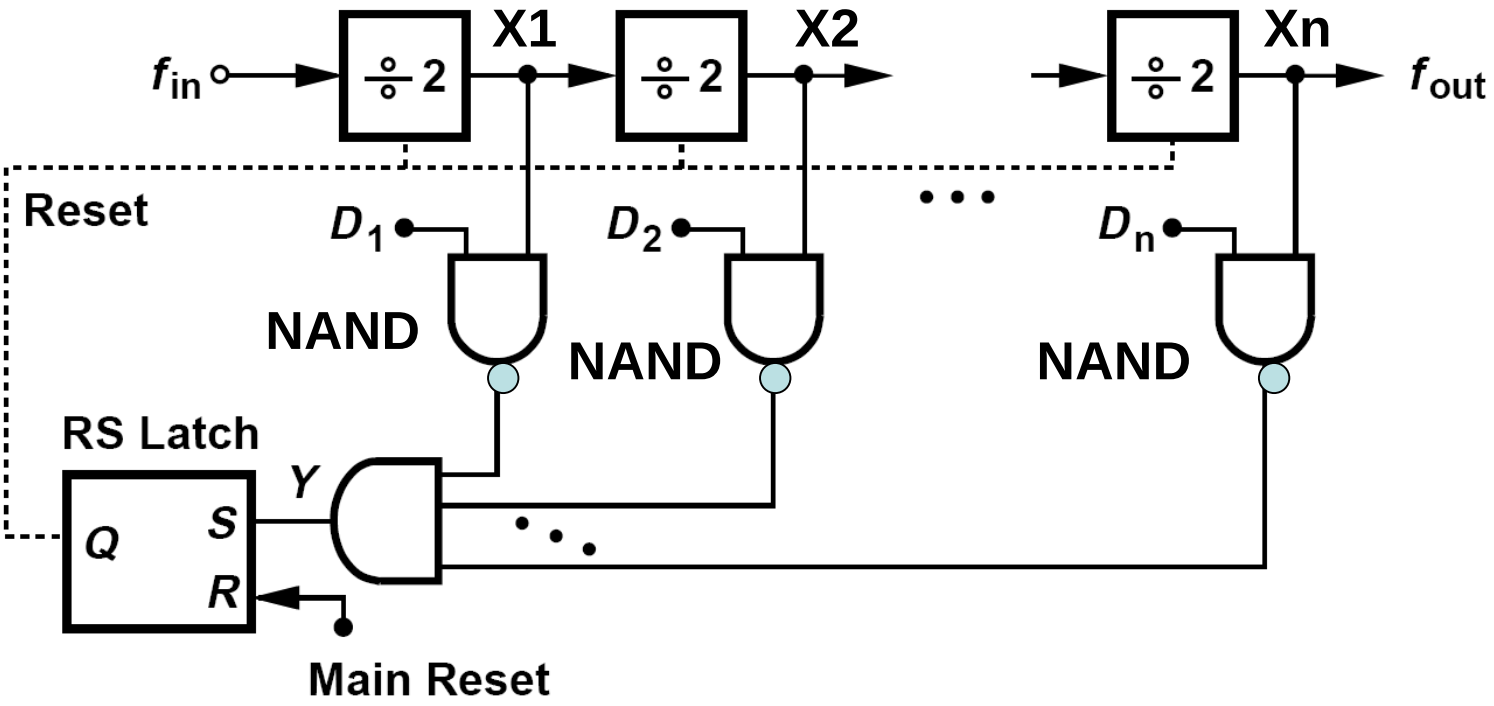


# Pulse Swallow Divider




- Sensing the high-frequency input, the prescaler proves the most challenging of the three building blocks.
- S(N+1)+(P-S)N=NP+S , P>S
- As a rule of thumb, dual-modulus prescalers are about a factor of two slower than ÷2 circuits

# Swallow Counter Realization

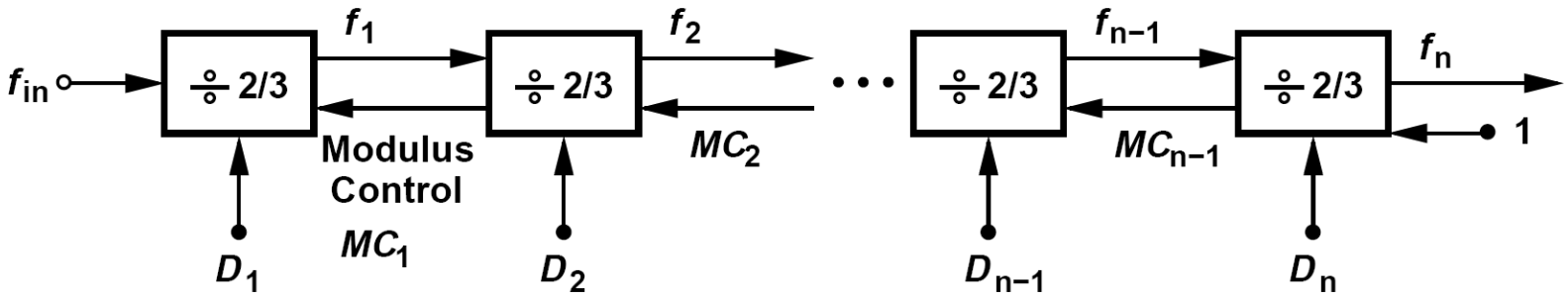



- The swallow counter is typically designed as an asynchronous circuit for the sake of simplicity and power saving

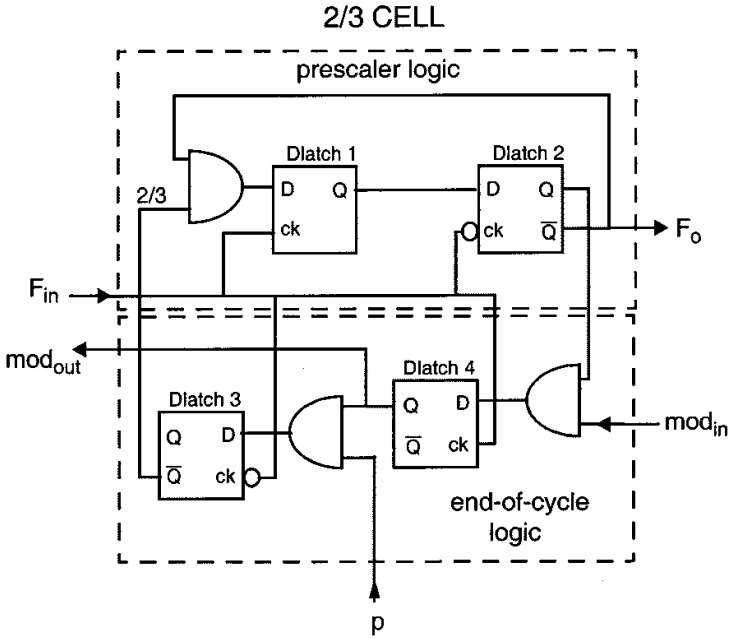
- initial [X4,..,X1]=[1111], [D4, ..,D1]=[1000]

  [X4,..,X1]=1111, 1110, 1101, 1100,1011, 1010,1001, 1000, 0111 –>Y=High

# Modular Divider Realizing Multiple Divider Ratios

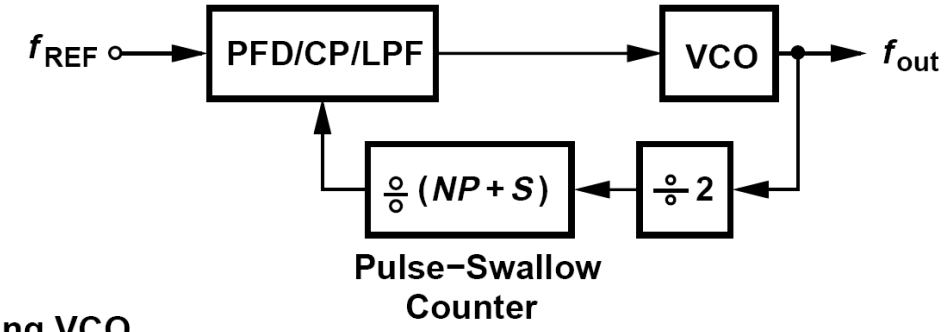


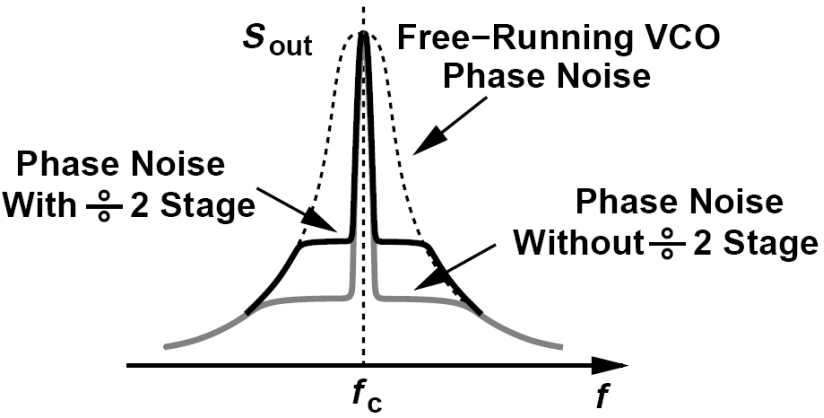

- **This method incorporates ÷2/3 stages in a modular form so as to reduce the design complexity. Each ÷2/3 block receives a modulus control from the next stage. The digital inputs set the overall divide ratio according to:**

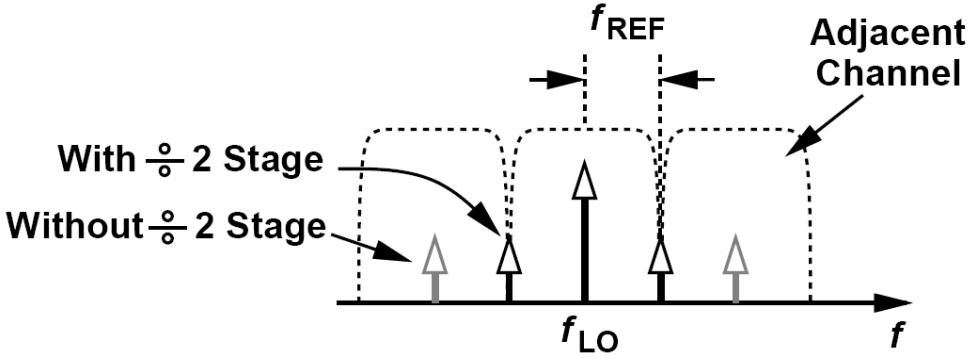



$$N = 2^n + D_n 2^{n-1} + D_{n-1} 2^{n-2} + \cdots + 2D_2 + D_1$$

# Example :Preceding the Pulse Swallow Divider by a ÷2



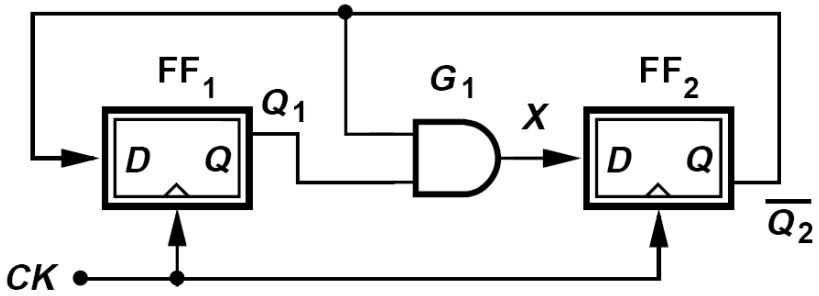




**Here, $f_{out} = 2(NP + S)f_{REF}$ . Thus, a channel spacing of $f_{ch}$ dictates $f_{REF} = f_{ch}/2$. The lock speed and the loop bandwidth are therefore scaled down by a factor of two, making the VCO phase noise more pronounced. One advantage of this approach is that the reference sideband lies at the edge of the adjacent channel rather than in the middle of it.**

# Divide-by-3 Divider

**Divide-by-3 Circuit:**

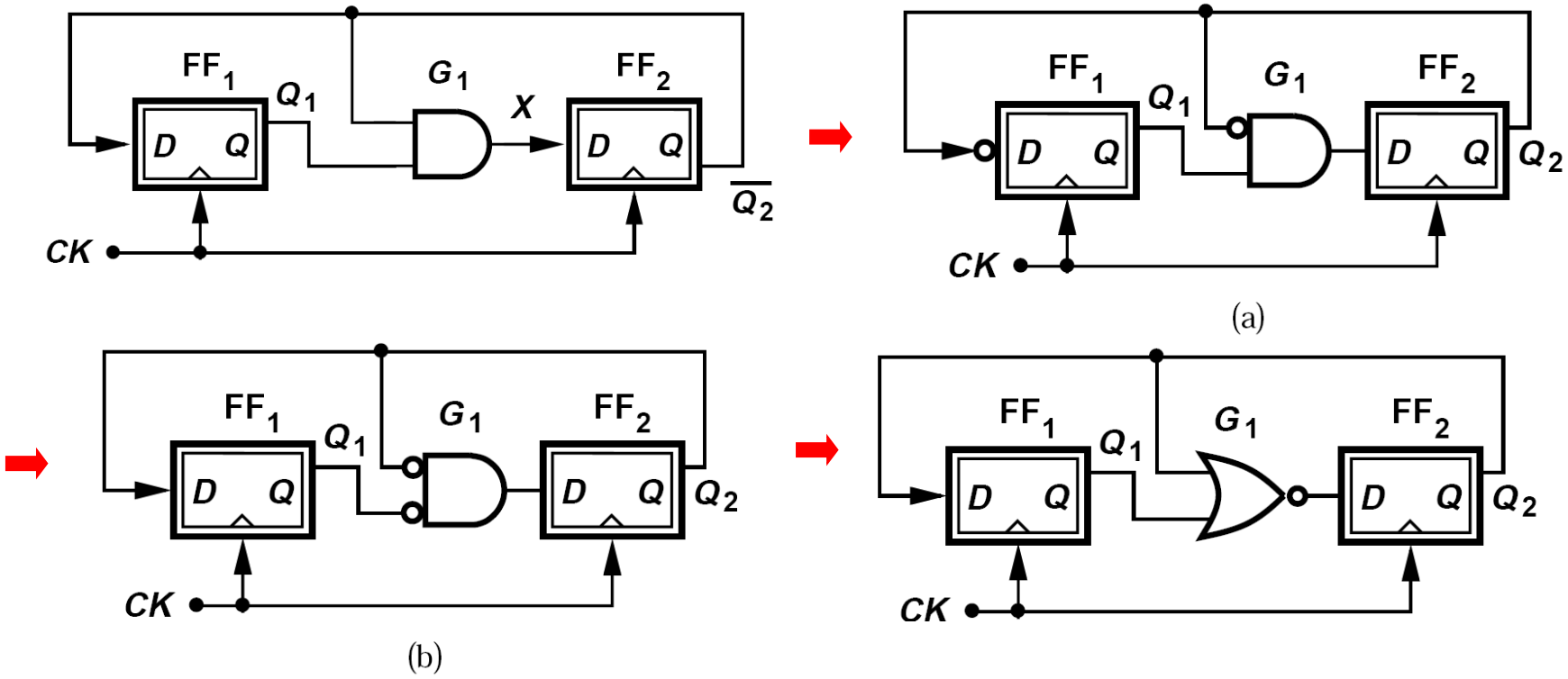



**Suppose the circuit begins with $Q_1\overline{Q}_2$ = 00. next three cycles, $Q_1\overline{Q}_2$ goes to 10, 11, and 01. Note that the state $Q_1\overline{Q}_2$ = 00 does not occur again because it would require the previous values of $\overline{Q}_2$ and $X$ to be ZERO and ONE, respectively.**

$$Q_1\overline{Q_2} = 00 \rightarrow X = 0 \rightarrow Q_2 = 0, \overline{Q_2} = 1 \rightarrow Q_1\overline{Q_2} = 01$$

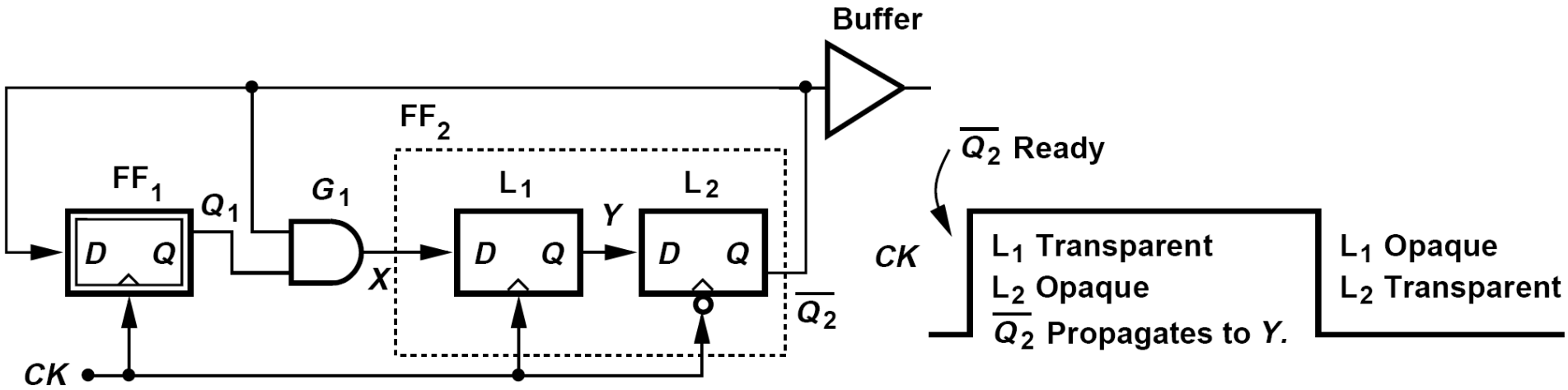
$$\rightarrow Q_1\overline{Q_2} = 11 \rightarrow X = 1 \rightarrow Q_2 = 1, \overline{Q_2} = 0 \rightarrow Q_1\overline{Q_2} = 10 \rightarrow Q_1\overline{Q_2} = 01$$

# Example : A ÷3 Circuit Using a NOR Gate rather than an AND Gate



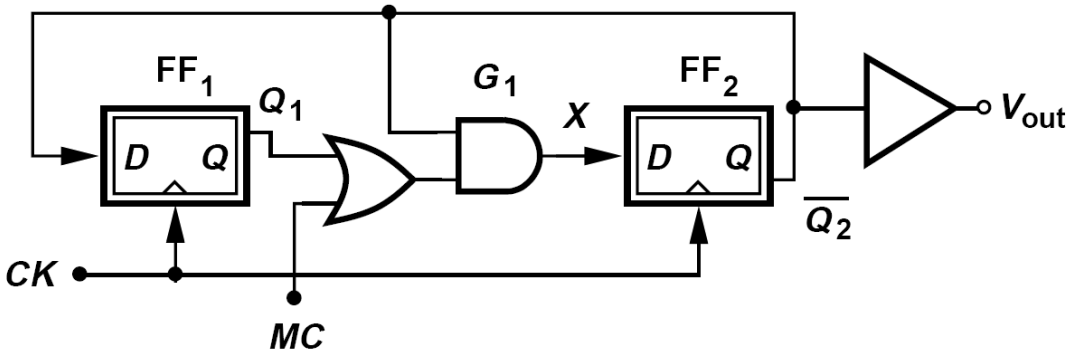

**The reader can prove that this circuit cycles through the following three states: $Q_1Q_2$ = 00; 01; 10.**

# Speed Limitation of the ÷3 Stage

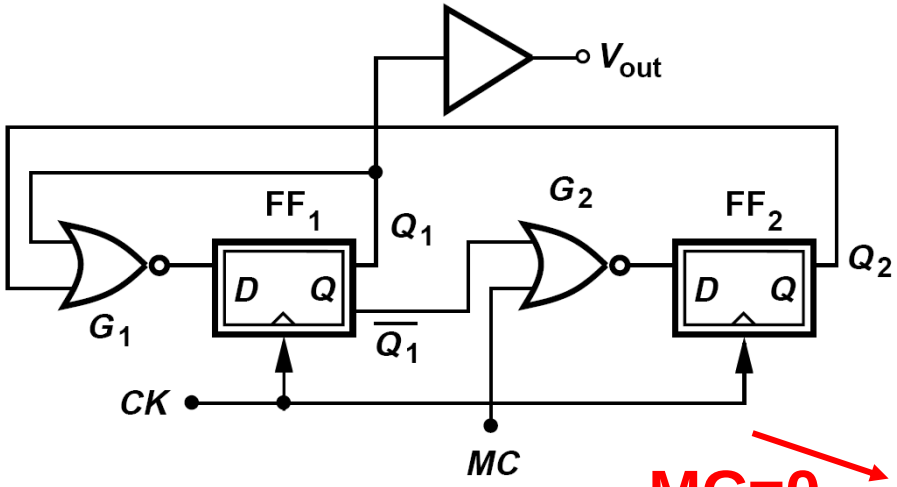



**Suppose *CK* is initially low, $L_1$ is opaque (in the latch mode), and $L_2$ is transparent (in the sense mode). When *CK* goes high and $L_1$ begins to sense, the value of $\overline{Q}_2$ must propagate through $G_1$ and $L_1$ before *CK* can fall again. Thus, the delay of $G_1$ enters the critical path. Moreover, $L_2$ must drive the input capacitance of $FF_1$, $G_1$, and an output buffer. These effects degrade the speed considerably, requiring that *CK* remain high long enough for $\overline{Q}_2$ to propagate to *Y* .**

# Divide-by-2/3 Circuits

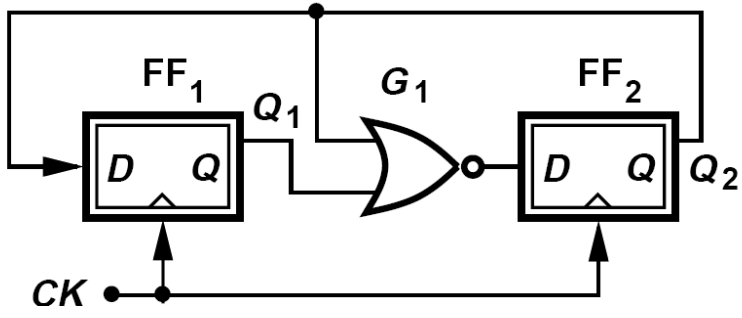



- The ÷2/3 circuit employs an OR gate to permit ÷3 operation if the modulus control, MC, is low or ÷2 operation if it is high.



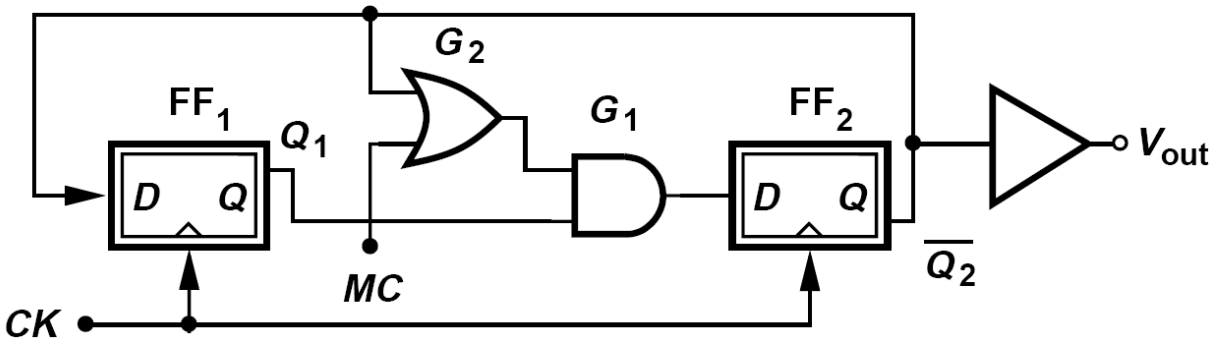

MC=0

- The output can be provided by only *FF*$_1$. This circuit has a 40% speed advantage over previous ÷2/3 circuit by reducing the loadings of FF2

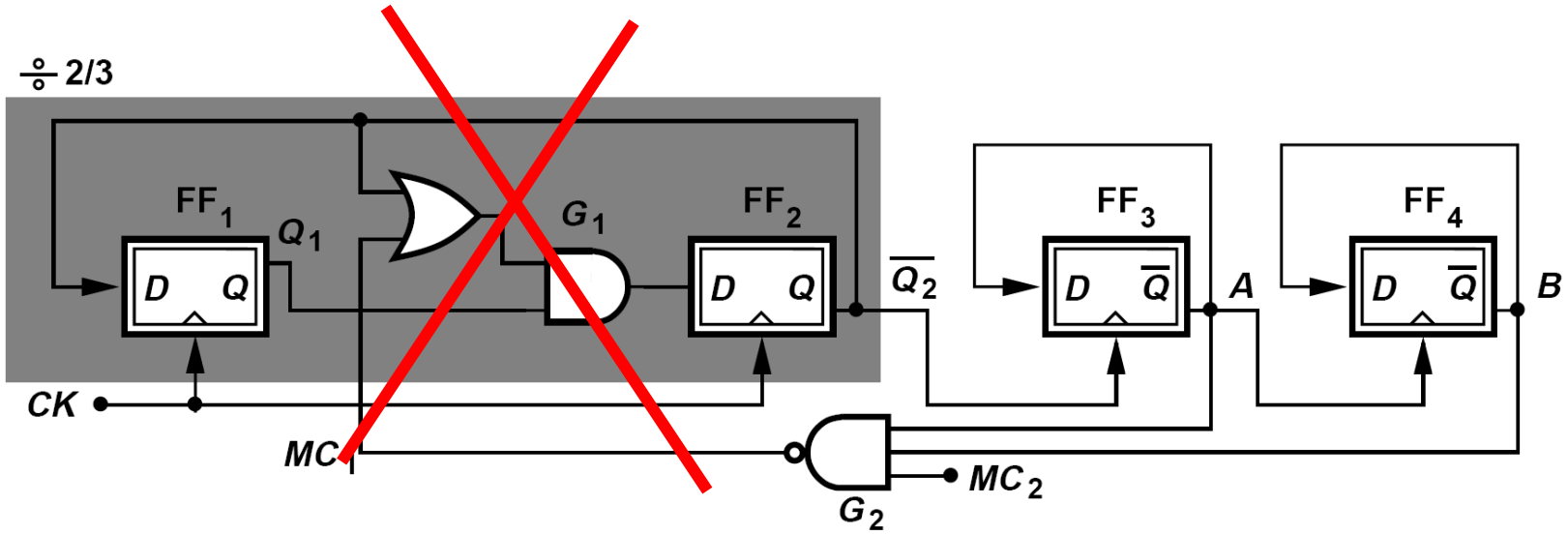



- MC=1, Q2=0, →DFF1 : Divide-by-two

# Divide-by-3/4 Circuit and Divide-by-8/9 Circuit

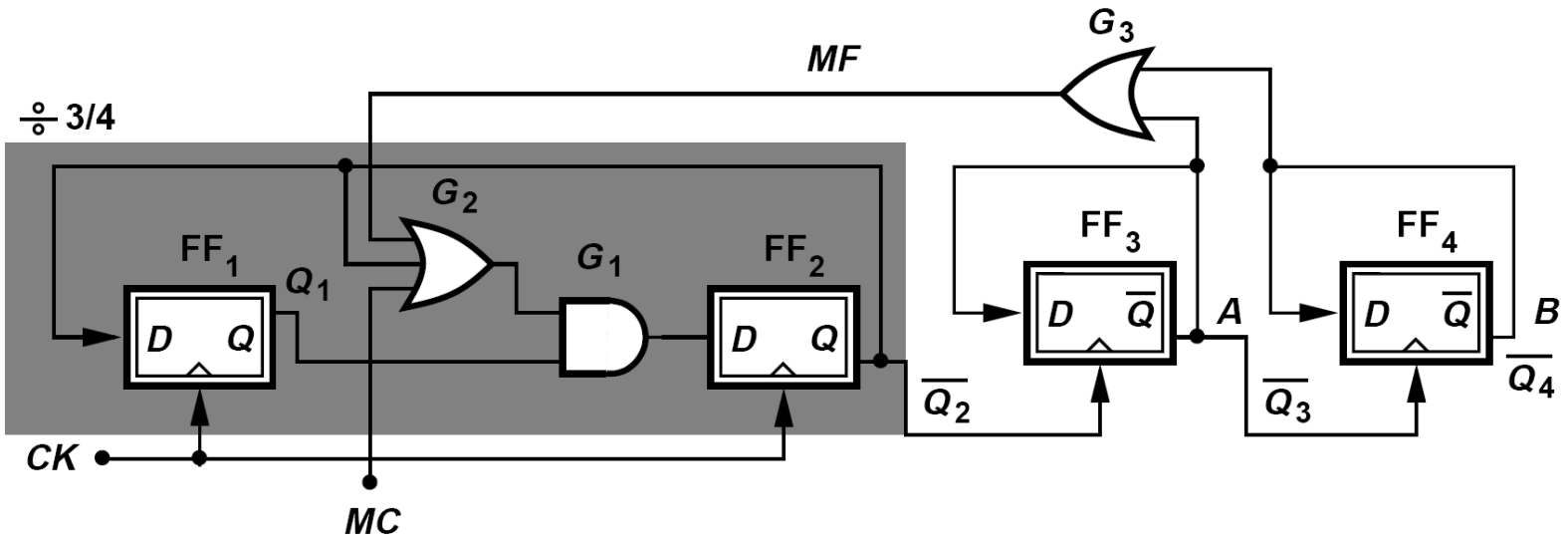



- When *MC*=1, the circuit divides by 4;
- If *MC*=0, it divides by 3




- If $MC_2$ is low, $MC_1$ is high, the overall circuit operates as a ÷8 circuit; if $MC_2$ is high, the circuit divides by 9.

# Example: a Divide-by-15/16 Circuit

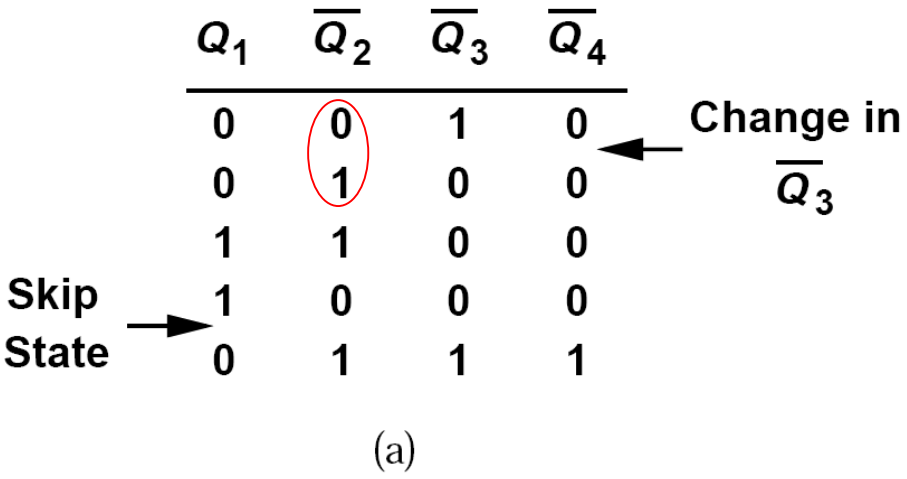


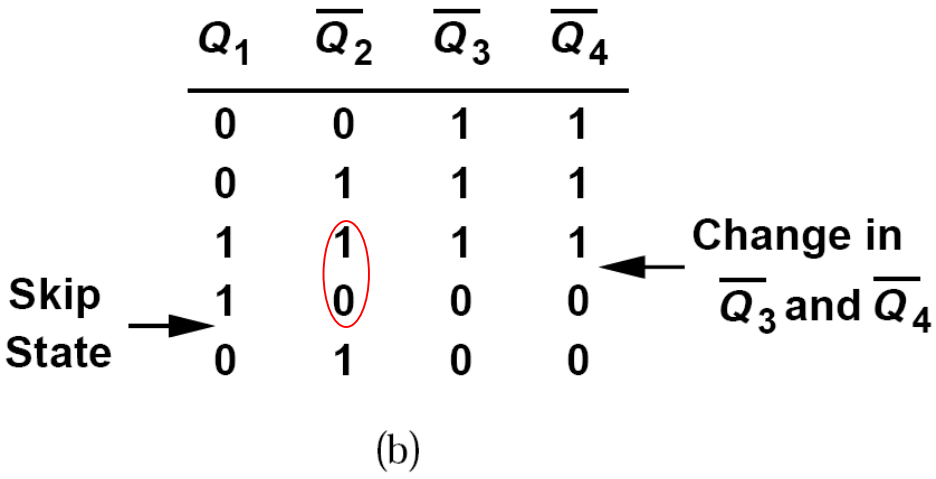

**Since the ÷3/4 stage (D34) divides by 4 when *MC* is high, we surmise that only two more ÷2 circuits must follow to provide ÷16. To create ÷15, we must force D34 to divide by 3 for one clock cycle. Shown in the figure above, the circuit senses the outputs of the asynchronous ÷2 stages by an OR gate and lowers *MF* when *AB* = 00. Thus, if *MC* is high, the circuit divides by 16. If *MC* is low and the ÷2 stages begin from 11, *MF* remains high and D34 divides by 4 until *AB* = 00. At this point, *MF* falls and D34 divides by 3 for one clock cycle before *A* goes high.**

*÷4 three times & ÷3 once*

*4x3+3x1=15*

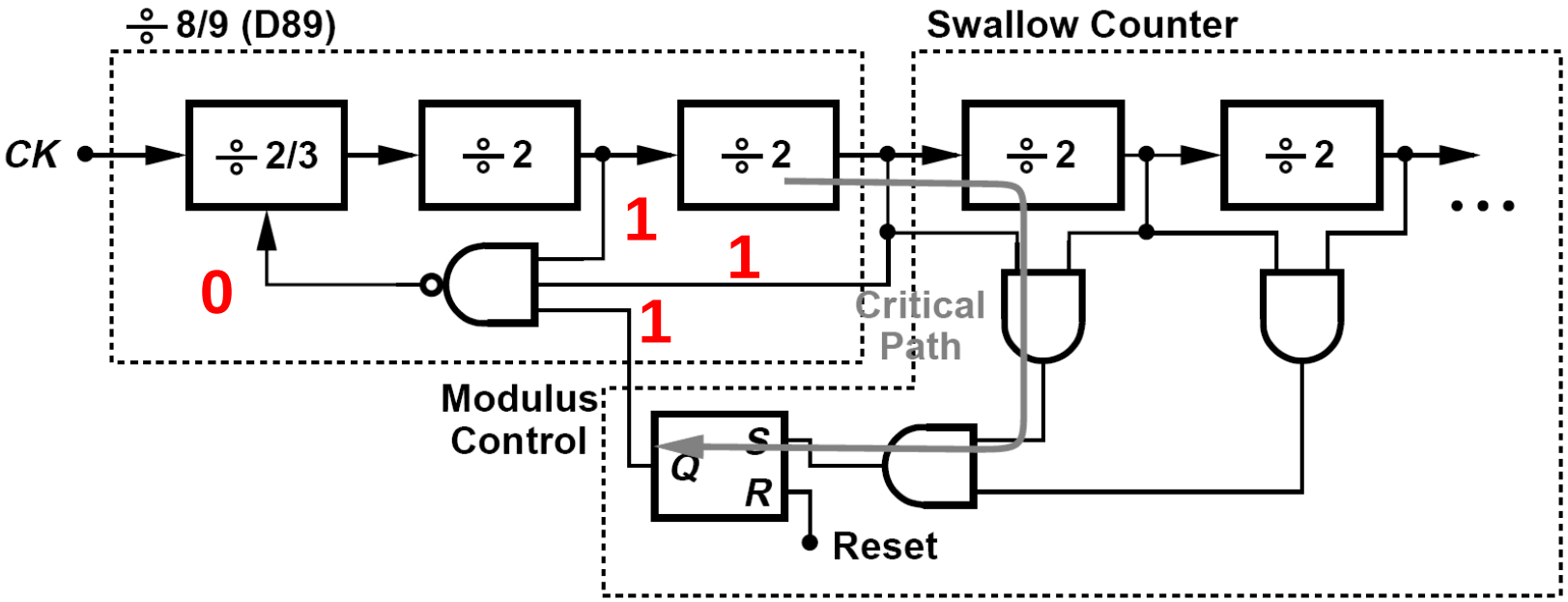
# Potential Race Conditions @Divide-by-15



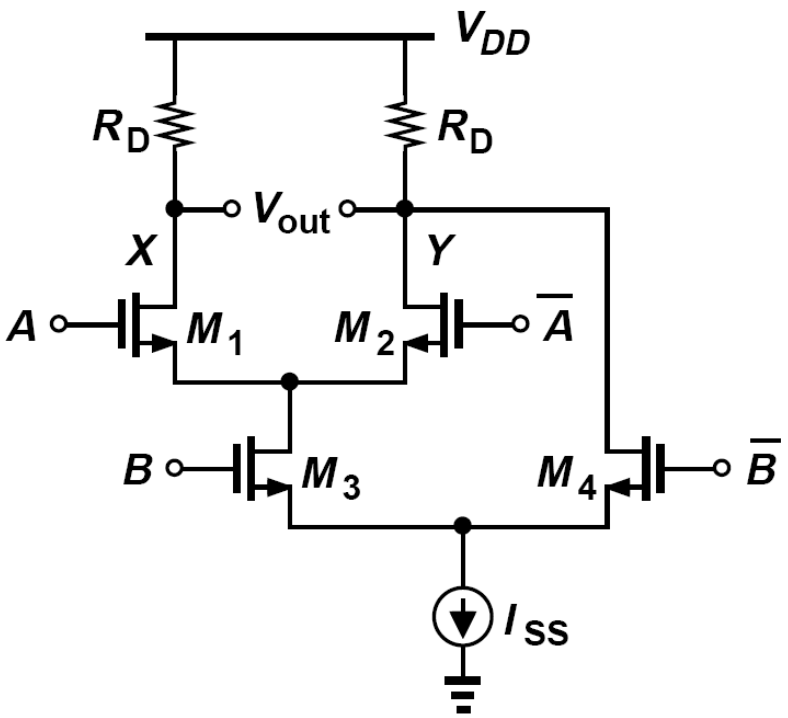

- First suppose $FF_3$ and $FF_4$ change their output state on the rising edge of their clock inputs. If MC is low, the circuit continues to divide by 16. As in (a), state 00 ($Q_1\overline{Q_2}$) is skipped. The propagation delay through $FF_3$ and $G_3$ need not be less than a cycle of $CK_{in}$
- In the case (b), $FF_3$ and $FF_4$ change their output state on the falling edge of their clock inputs, the ÷3/4 circuit must skip the state 00. The delay through $FF_3$, $FF_4$, and $G_3$ should be less than half of a $CK_{in}$ cycle. This is in general difficult to achieve and demands higher power dissipation. Thus the first choice is preferable.

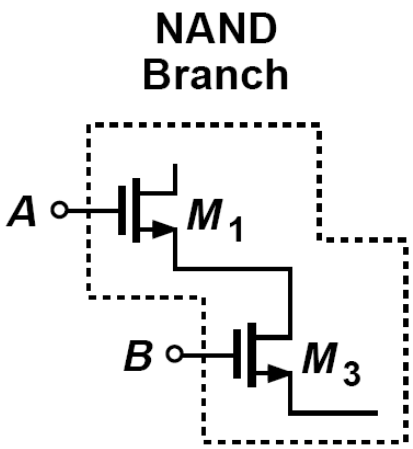
# Example : Choice of Prescaler Modulus

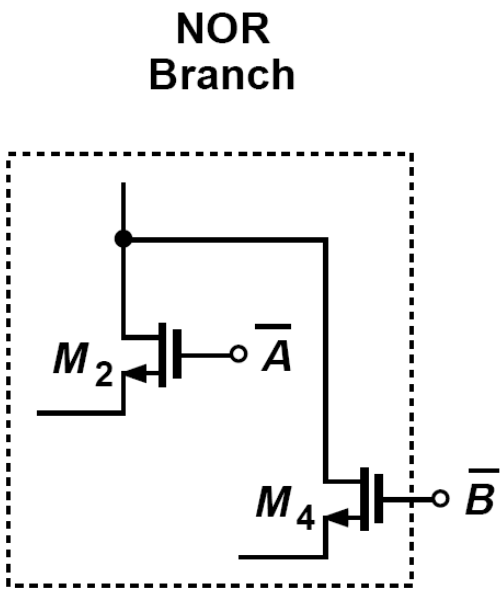



- The last pulse generated by the prescaler in the previous ÷8 mode (just before the ÷9 mode begins) must propagate through the first ÷2 stage in the swallow counter, the subsequent logic, and the RS latch in fewer than seven input cycles.
- A large N for the prescaler permits a long delay for an asynchronous stages and feedback loop, but it leads a higher power.

# Divider Logic Styles-Current Steering Circuit

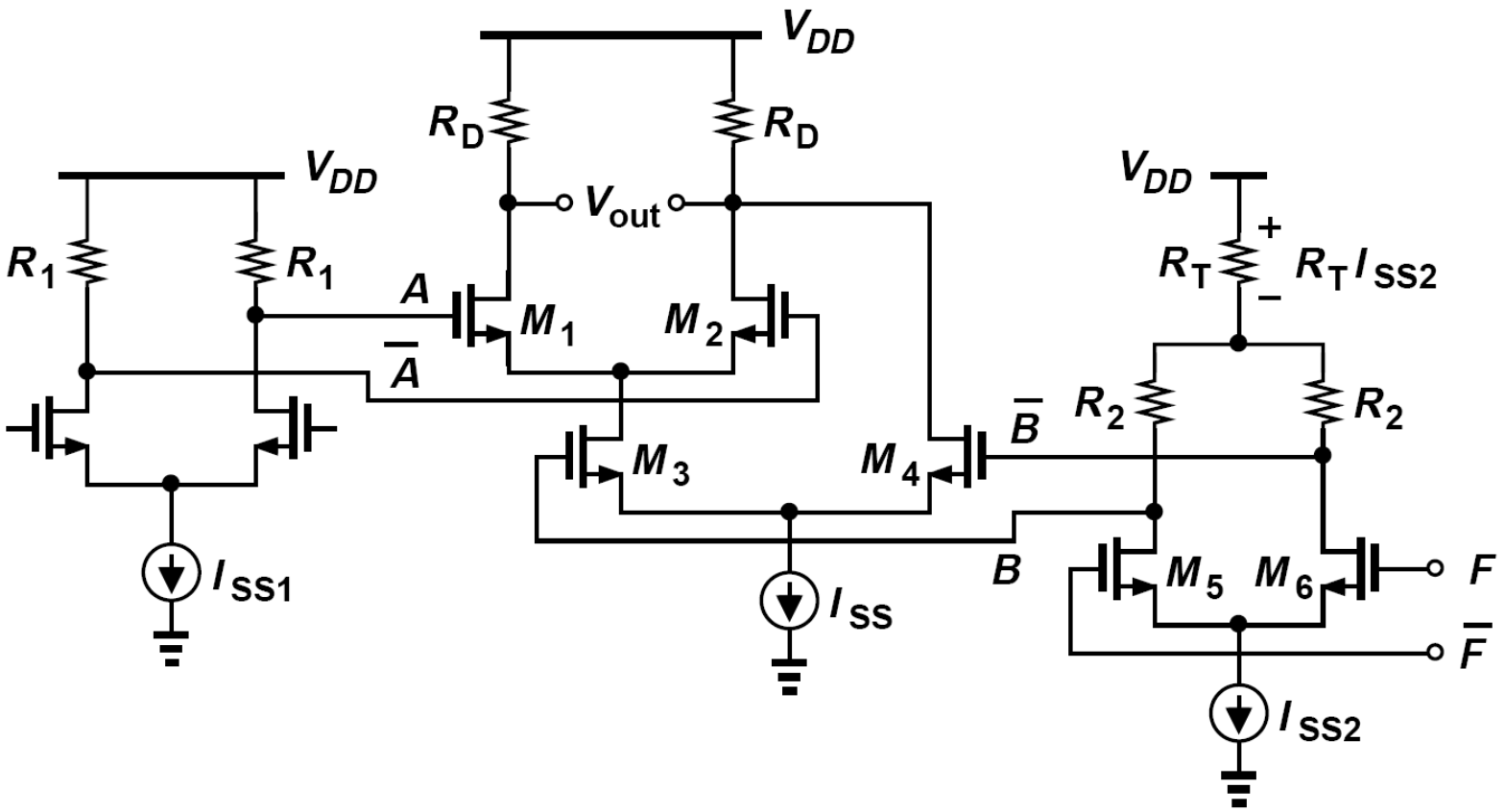


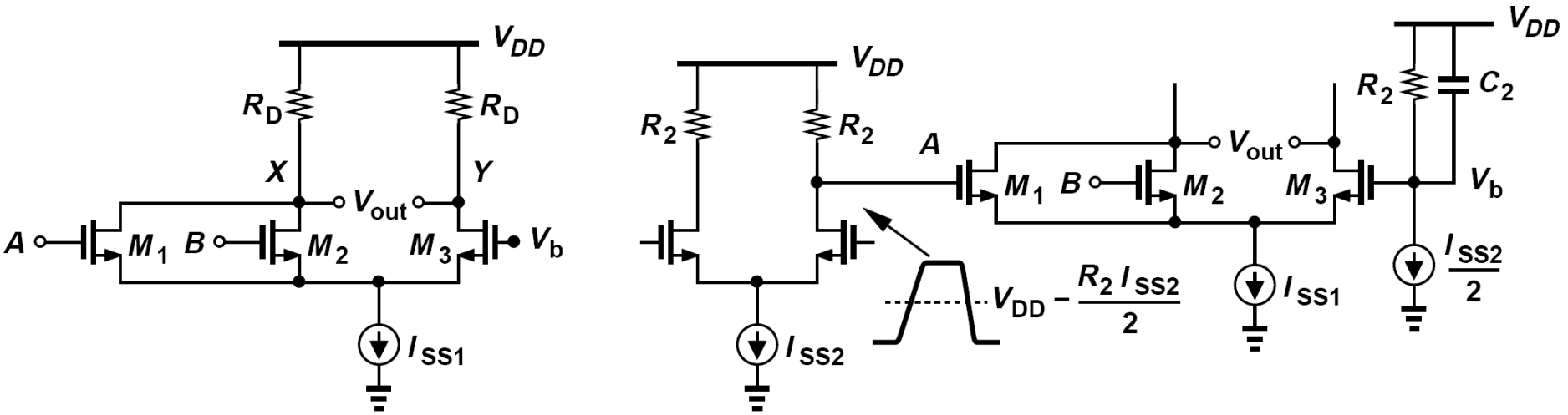

- CML operates with moderate input and output swings, and provides differential outputs and hence a natural inversion.
- The circuit above is typically designed for a single-ended output swing of $R_D I_{SS}$ = 300mV, and the transistors are sized such that they experience complete switching with such input swings

# Problem of Common-Mode Compatibility at NAND Inputs



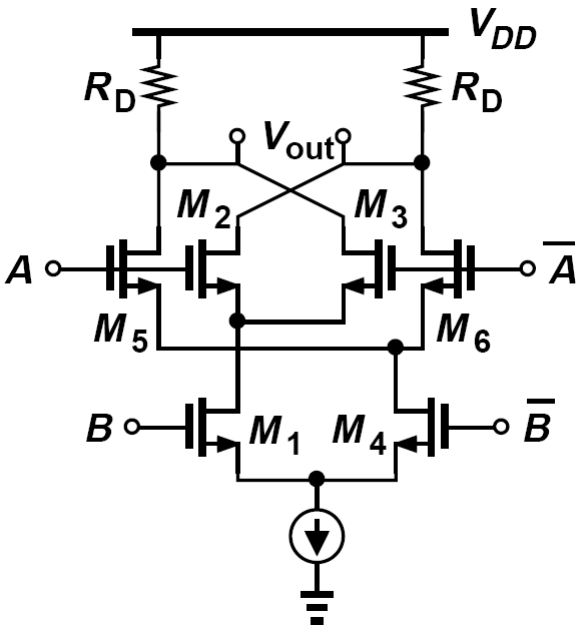

- A and /A swing : $V_{DD}$ and $V_{DD}$-$I_{SS1}R_1$
- B and /B swing: $V_{DD} – R_T I_{SS2} - R_2 I_{SS2}$ and $V_{DD} - R_T I_{SS2}$
- The high level of *F* and *F* does not exceed $V_{DD} – R_T I_{SS2} - R_2 I_{SS2} + V_{TH}$ if $M_5$ and $M_6$ must not enter the triode region

# Choice at Low Supply Voltages

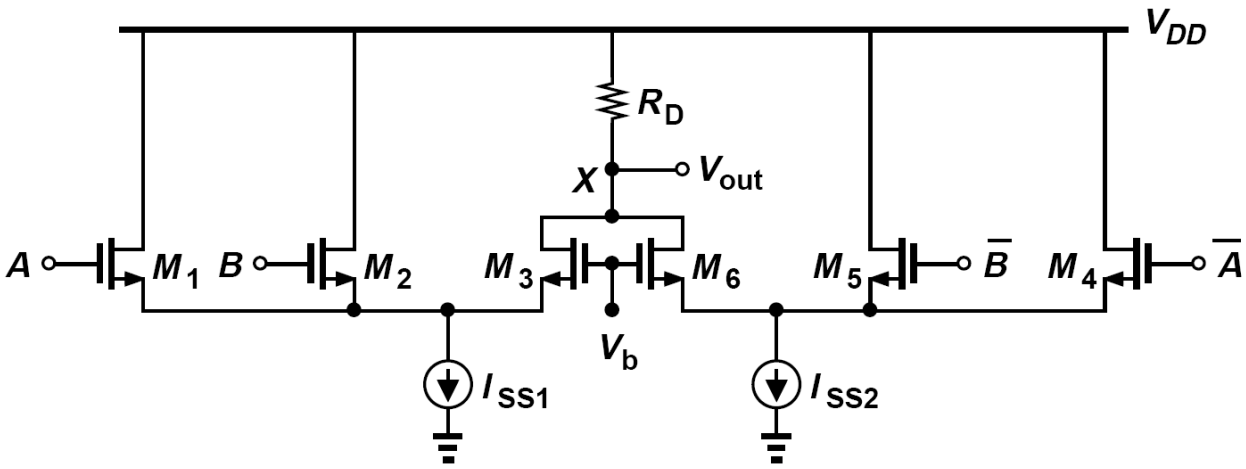



- The CML NOR/OR gate, avoid stacking. This stage operates only with single-ended inputs.
- the worst case occurs if only *M1* or *M2* is on. Thus, for either transistor to "overcome" *M3*, we require that the widths $W1 = W2 \geq W3$.

# CML XOR Implementation



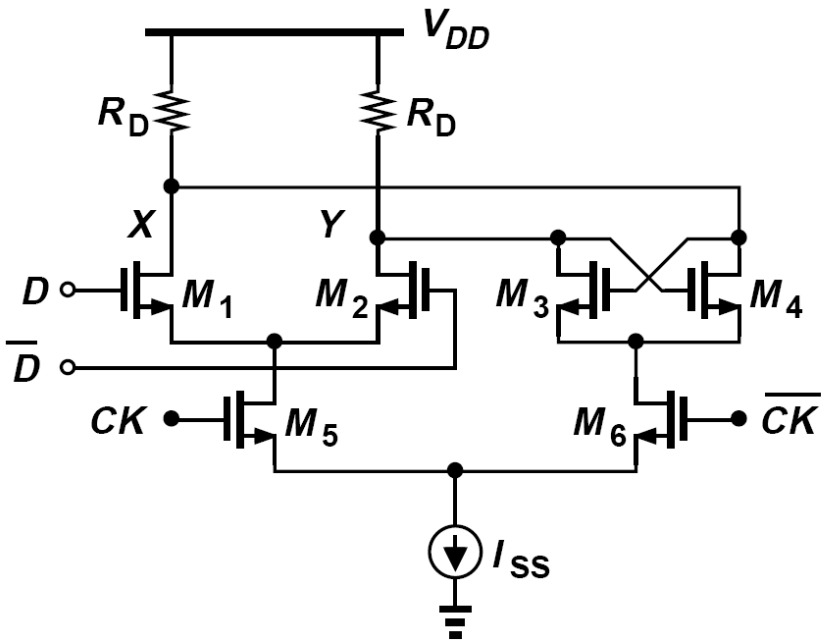

- The topology is identical to the Gilbert cell mixer. As with the CML NAND gate, this circuit requires proper CM level shift and does not easily operate with low supply voltages.

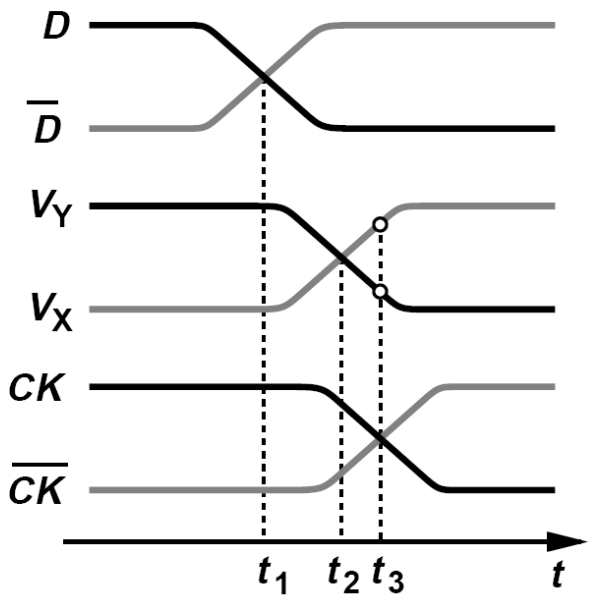



- Symmetric low-voltage XOR gate.

$$V_{out} = \overline{(\overline{A+B}+\overline{A}+\overline{B})}$$
$$= \overline{A}B + A\overline{B}.$$

# Speed Attributes of CML Latch

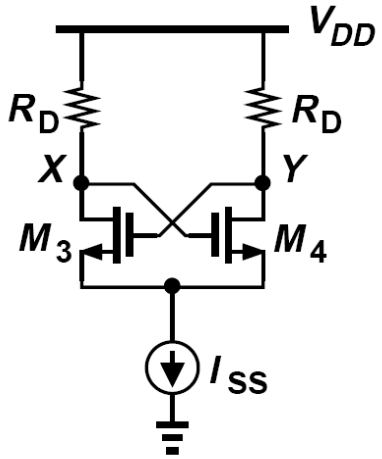


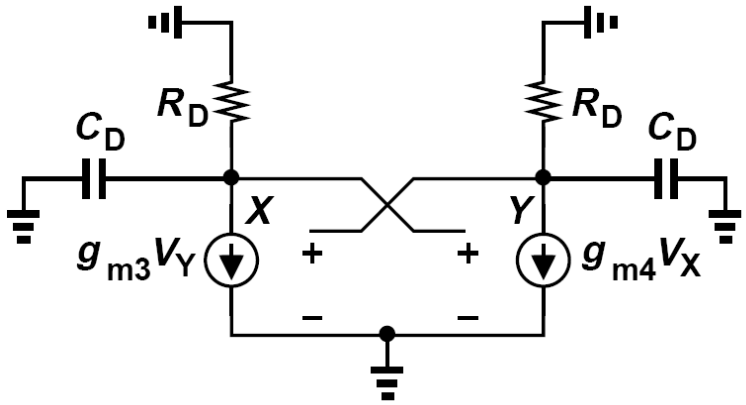

- Speed advantage of CML circuits is especially pronounced in latches.
- The latch operates properly even with a limited bandwidth at *X* and *Y* if (a) in the sense mode $V_X$ and $V_Y$ begin from their full levels and cross, and (b) in the latch mode, the initial difference between $V_X$ and $V_Y$ can be amplified to a final value of $I_{SS}R_D$

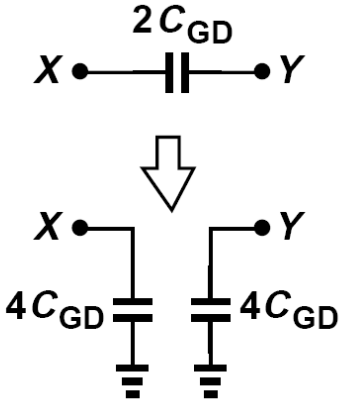
# Example : Regenerative Amplification (I)

**Regeneration mode**




**Small-signal Model**



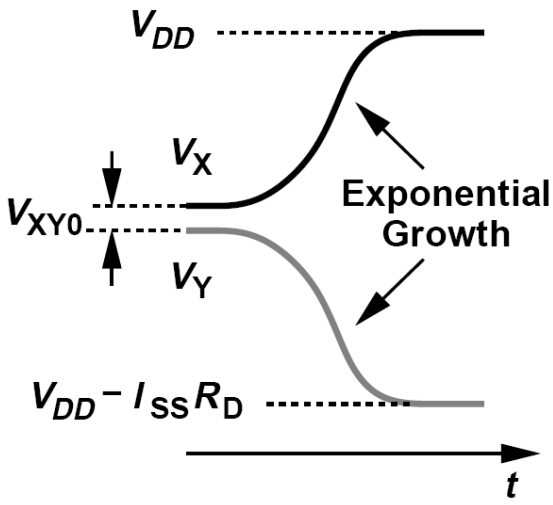




**If $V_{XY0}$ is small, $M_3$ and $M_4$ are near equilibrium and the small-signal equivalent circuit can be constructed as shown above. Here, $C_D$ represents the total capacitance seen at $X$ and $Y$ to ground, including $C_{GD1} + C_{DB1} + C_{GS3} + C_{DB3} + 4C_{GD3}$ and the input capacitance of the next stage. The gate-drain capacitance is multiplied by a factor of 4 because it arises from both $M_3$ and $M_4$ and it is driven by differential voltages. Writing a KCL at node $X$ gives**

$$\frac{V_X}{R_D} + C_D\frac{dV_X}{dt} + g_{m3,4}V_Y = 0$$

# Example to Formulate Regenerative Amplification (II)

**Similarly,** $\frac{V_Y}{R_D} + C_D\frac{dV_Y}{dt} + g_{m3,4}V_X = 0$



(c)

**Subtracting and grouping the terms, we have**

$$-R_DC_D\frac{d(V_X - V_Y)}{dt} = (1 - g_{m3,4}R_D)(V_X - V_Y)$$

**We denote $V_X$ - $V_Y$ by $V_{XY}$ , divide both sides by $-R_DC_DV_{XY}$ , multiply both sides by $dt$, and integrate with the initial condition $V_{XY}$ ($t$ = 0) = $V_{XY0}$. Thus,**

$$V_{XY} = V_{XY0}\exp\frac{(g_{m3,4}R_D - 1)t}{R_DC_D}$$

**Interestingly, $V_{XY}$ grows exponentially with time, exhibiting a "regeneration time constant" of**

$$\tau_{reg} = \frac{R_DC_D}{g_{m3,4}R_D - 1}$$

**Of course, as $V_{XY}$ increases, one transistor begins to turn off and its $g_m$ falls toward zero. Note that, if $g_{m3,4}R_D >> 1$, then $\tau_{reg} \approx C_D/g_{m3,4}$.**

# Example to Derive Relation Between Circuit Parameters and Clock Period

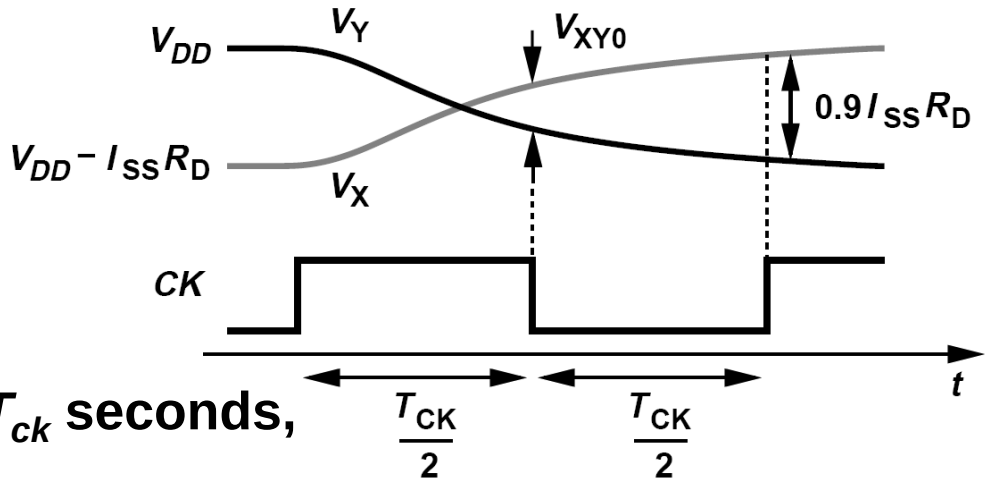
**Initial voltage difference**

$$V_{XY0} = 0.9 I_{SS} R_D \exp \frac{-0.5 T_{ck}}{\tau_{reg}} \quad (10.45)$$

**The minimum initial voltage must be established by the input differential pair in the sense mode [just before t = t3]. In the worst case, when the sense mode begins, $V_X$ and $V_Y$ are at the opposite extremes and must cross and reach $V_{XY0}$ in $0.5T_{ck}$ seconds. For example, $V_Y$ begins at $V_{DD}$ and falls according to**

$$V_Y(t) = V_{DD} - I_{SS} R_D \left(1 - \exp \frac{-t}{R_D C_D}\right)$$

$$V_X(t) = V_{DD} - I_{SS} R_D \exp \frac{-t}{R_D C_D}$$



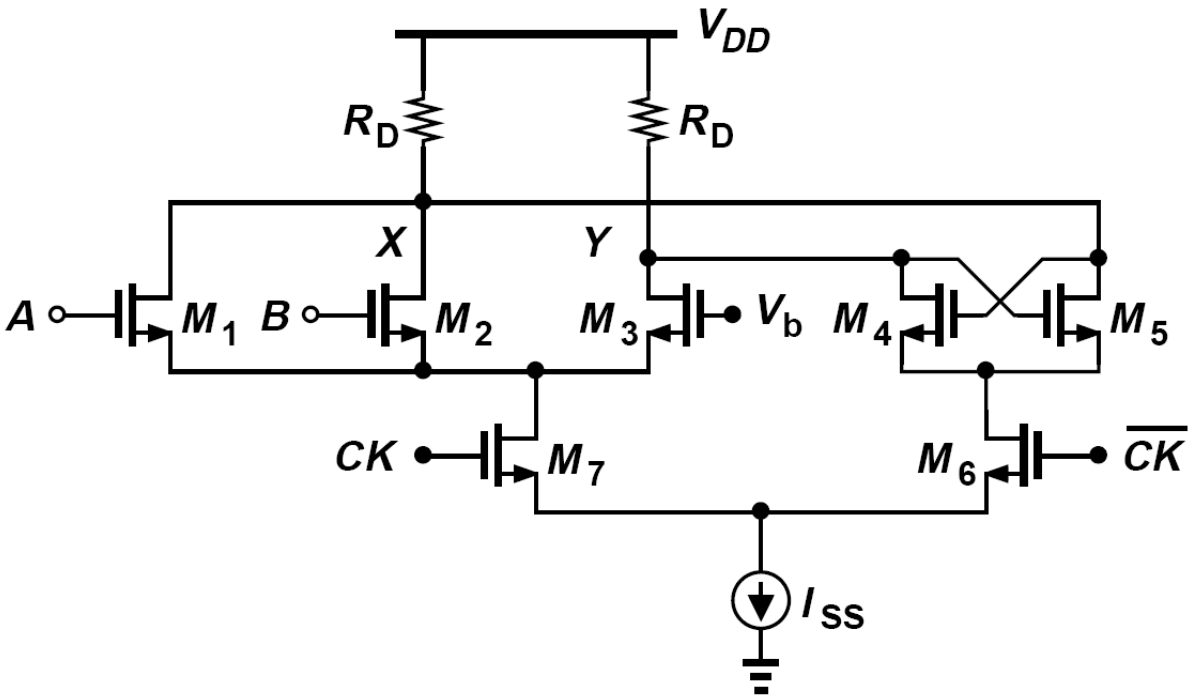

**Since $V_X$ - $V_Y$ must reach $V_{XY0}$ in $0.5T_{ck}$ seconds, we have**

$$-2 I_{SS} R_D \exp \frac{-0.5 T_{ck}}{R_D C_D} + I_{SS} R_D = 0.9 I_{SS} R_D \exp \frac{-0.5 T_{ck}}{\tau_{reg}}$$

$$\Rightarrow \quad 0.9 \exp \frac{-0.5 T_{ck}}{\tau_{reg}} + 2 \exp \frac{-0.5 T_{ck}}{R_D C_D} = 1 \quad \Rightarrow$$

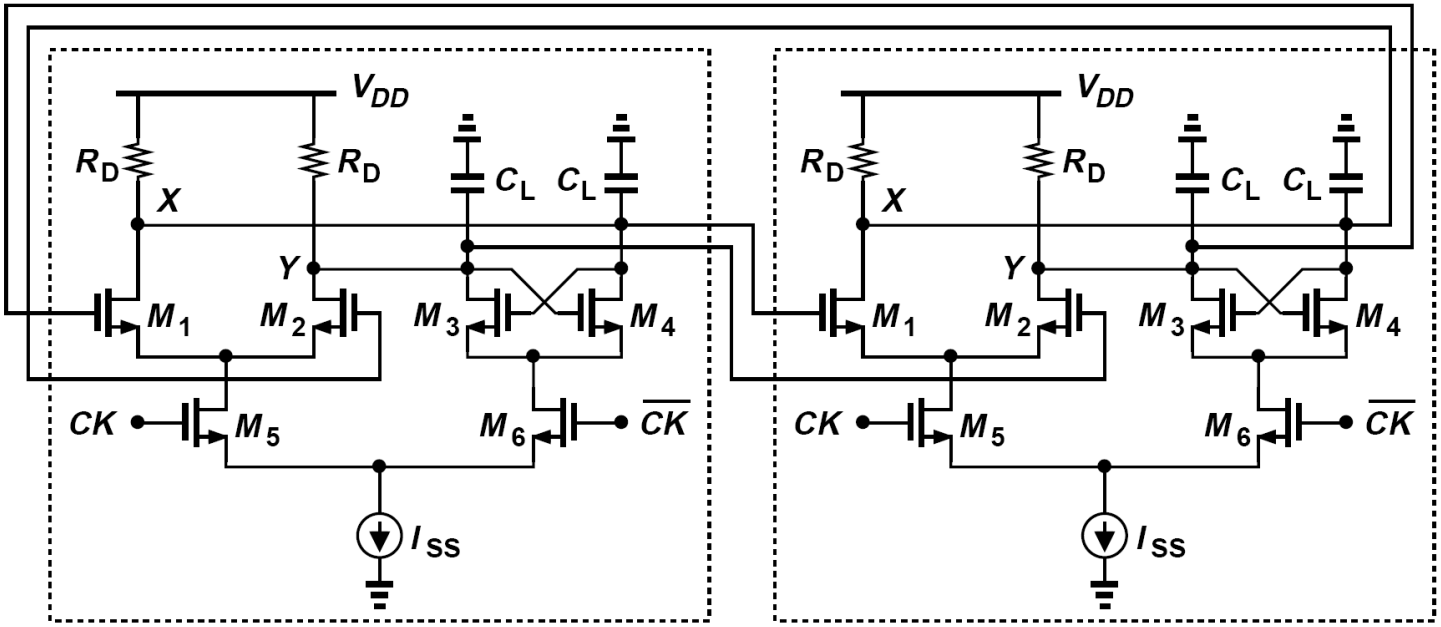
**It limits the upper value of $R_D C_D$ and the lower one of $g_{m3,4}$.**

# Merging Logic with Latch




- It is possible to merge logic with a latch, thus reducing both the delay and the power dissipation. For example, the NOR and the master latch of $FF_1$ depicted in previous high-speed divide-by-2/3 circuit can be realized as shown above. The circuit performs a NOR/OR operation on *A* and *B* in the sense mode, and stores the result in the latch mode.

# Design Procedure




**(1)Select $I_{SS}$ based on the power budget ; (2)Select $R_D I_{SS} \approx 300$mV**

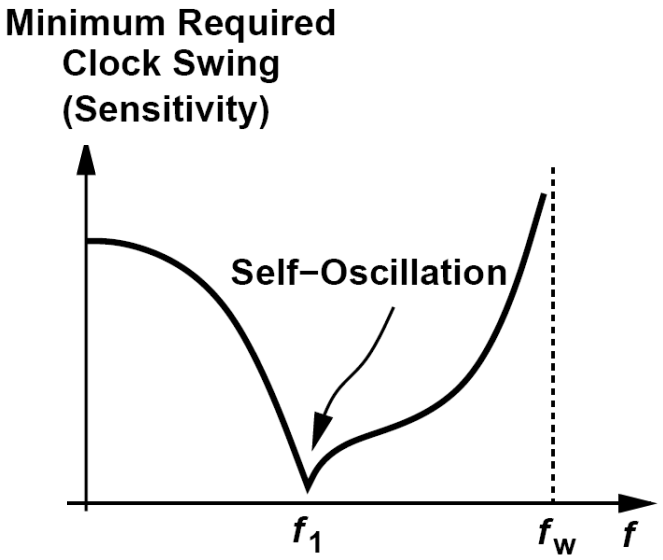
**(3)Select $(W/L)_{1,2}$ such that the diff. pair experiences nearly complete switching for a diff. input of 300mV**

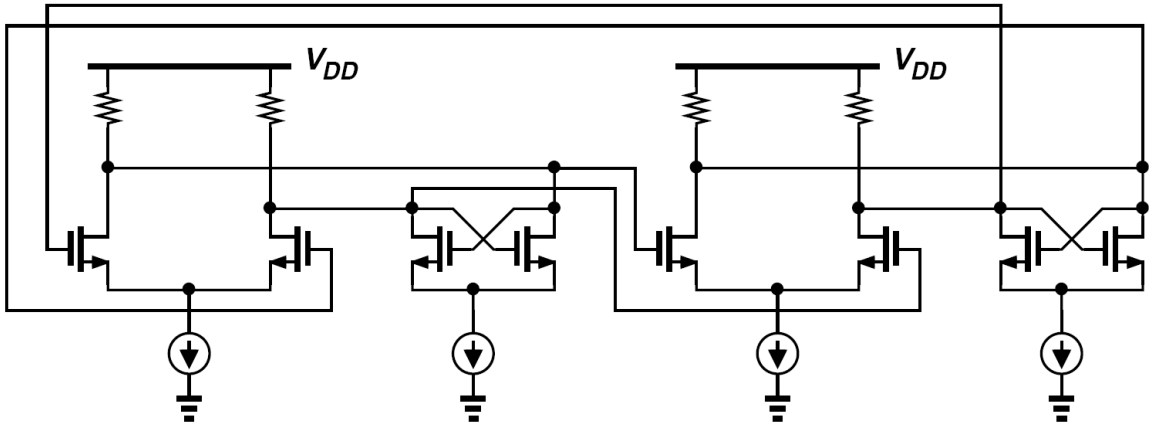
**(4)Select $(W/L)_{3,4}$ so that small-signal gain around regenerative loop exceeds unity**

**(5)Select $(W/L)_{5,6}$ such that the clocked pair steers most of the tail current with the specified clock swing**

# Example : Sensitivity of the ÷2 Circuit

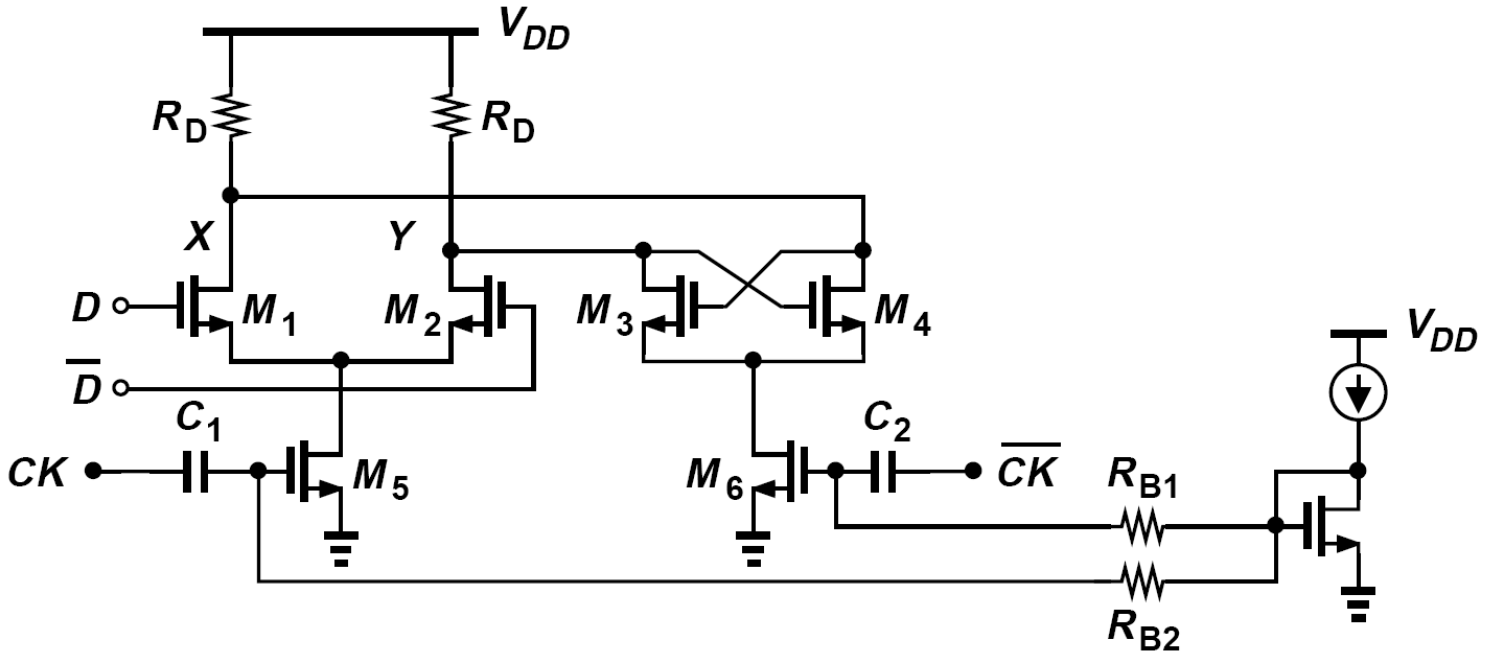
**The performance of high-speed dividers is typically characterized by plotting the minimum required clock voltage swing ("sensitivity") as a function of the clock frequency.**



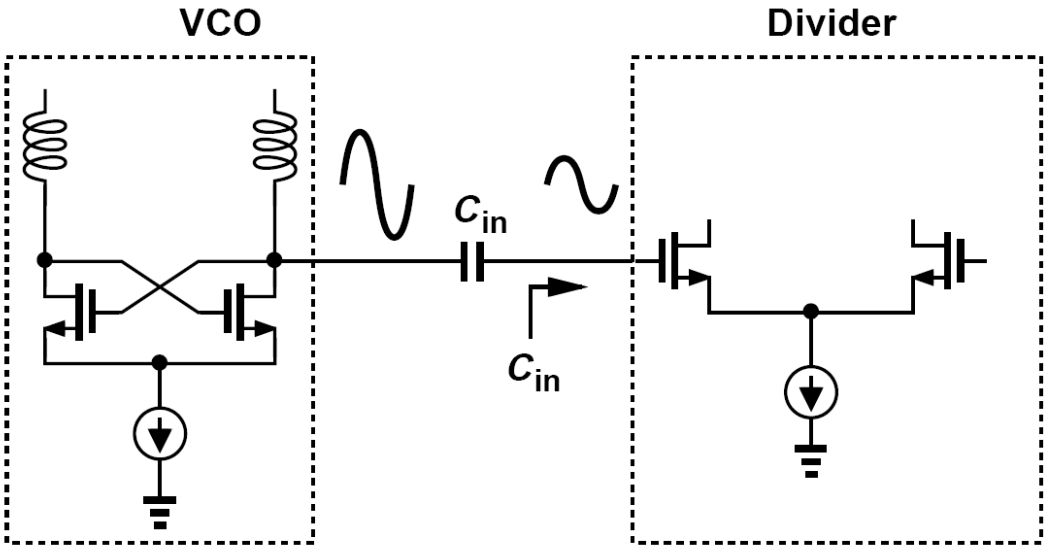

**For square clock waveforms, a small swing fails to steer all of the tail current, thereby keeping $M_1$-$M_2$ and $M_3$-$M_4$ simultaneously on. The circuit may therefore oscillate at $f_1/2$ (or injection-pulled by the clock).**
**The "self-oscillation" of the divider also proves helpful in the design process: We thus first test the circuit with a zero clock swing to ensure that it oscillates.**

# Class-AB Latch




- The bias of the clocked pair is defined by a current mirror and the clock is coupled capacitively.
- Large clock swings allow transistors $M_5$ and $M_6$ to operate in the class AB mode, i.e., their peak current well exceed their bias current. This attribute improves the speed of the divider.

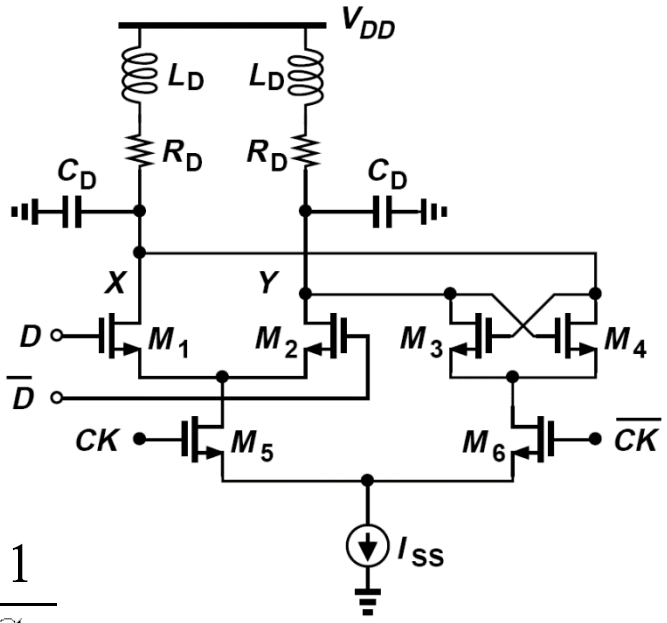
# Example : Choosing Coupling Capacitance



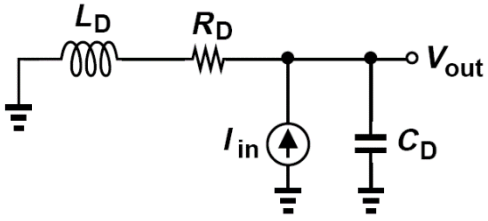

**Suppose the VCO output swing is twice that required by the divider. We simply choose each coupling capacitor to be equal to the input capacitance of the divider. This minimizes the size of the coupling capacitors, the load capacitance seen by the VCO (half of the divider input capacitance), and the effect of divider input capacitance variation on the VCO.**

# CML Using Inductive Peaking (Shunt Peaking)

$$\frac{V_{out}}{I_{in}} = \frac{L_D s + R_D}{L_D C_D s^2 + R_D C_D s + 1}$$




(a)




(b)

**Rewrite this as**

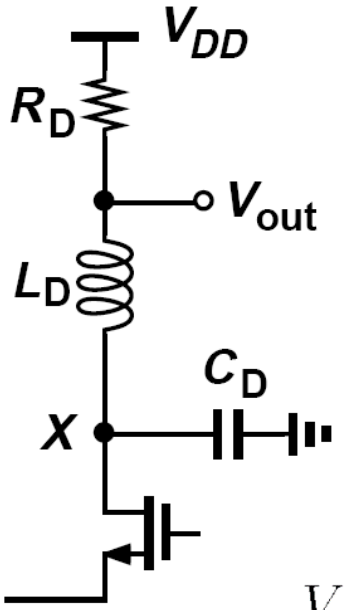
$$\frac{V_{out}}{I_{in}} = \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{1}{C_D}$$

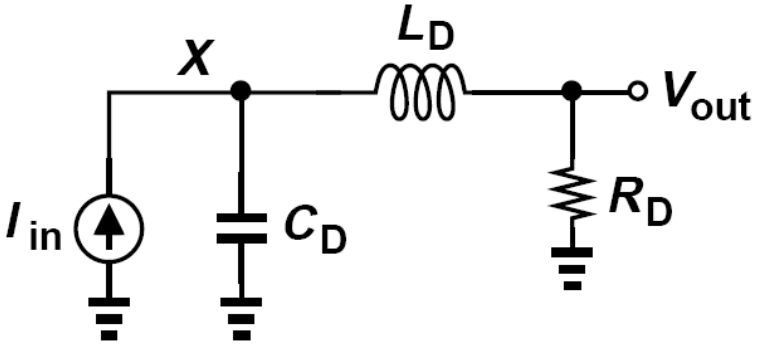
**where** $\zeta = \frac{R_D}{2}\sqrt{\frac{C_D}{L_D}} \qquad \omega_n = \frac{1}{\sqrt{L_D C_D}}$

**To determine the -3 dB bandwidth:** $$\frac{\omega_{-3dB}^2 + 4\zeta^2\omega_n^2}{(\omega_{-3dB}^2 - \omega_n^2)^2 + 4\zeta^2\omega_n^2\omega_{-3dB}^2} = \frac{2\zeta^2}{\omega_n^2}$$

**It follows that** $$\omega_{-3dB}^2 = \left[-2\zeta^2 + 1 + \frac{1}{4\zeta^2} + \sqrt{\left(-2\zeta^2 + 1 + \frac{1}{4\zeta^2}\right)^2 + 1}\right]\omega_n^2$$

# Series Peaking




$$\frac{V_{out}}{I_{in}}(s) = \frac{R_D}{L_D C_D s^2 + R_D C_D s + 1}$$

$$\zeta = \frac{R_D}{2}\sqrt{\frac{C_D}{L_D}}$$

$$\omega_n = \frac{1}{\sqrt{L_D C_D}}$$

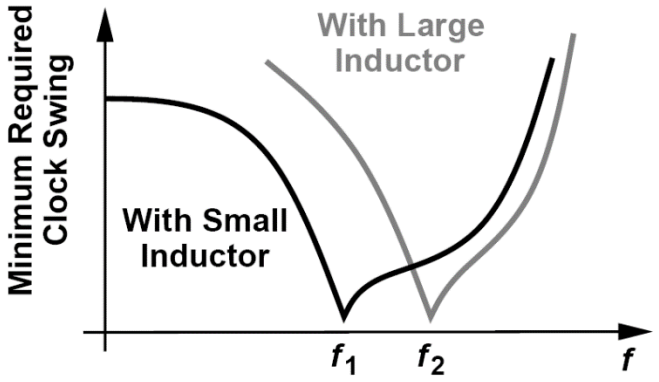
**The -3 dB bandwidth is computed as**

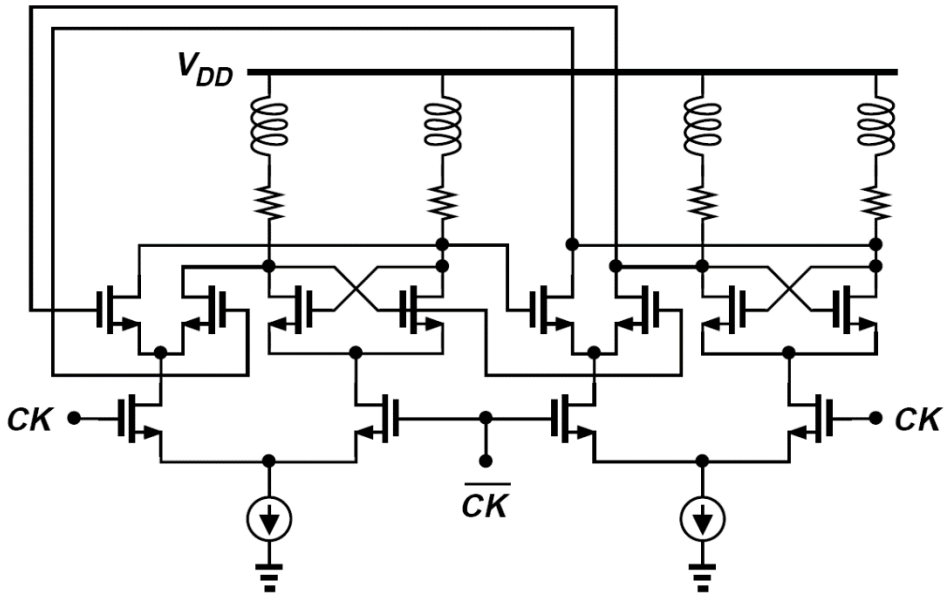
$$\omega_{-3dB}^2 = [-(2\zeta^2 - 1) + \sqrt{(2\zeta^2 - 1)^2 + 1}]\omega_n^2,$$

If $\zeta = 1/\sqrt{2}$, $\omega_{-3dB} = \omega_n = \sqrt{2}/(R_D C_D)$

- **Series peaking increases the bandwidth by about 40%**

# Inductively-peaked Latch

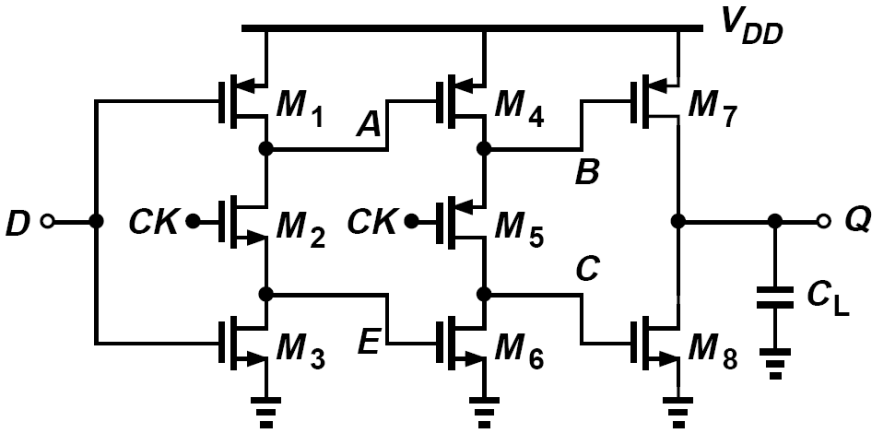


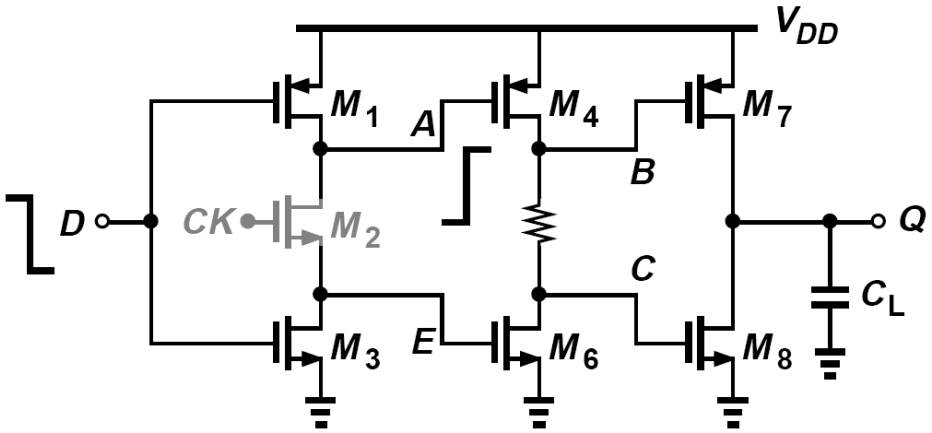




- As the value of $L_D$ becomes large enough, the circuit begins to fail at low frequencies. This is because the circuit approaches a quadrature LC oscillator that is injection-locked to the input clock
- $Q=L_D \omega / R_D$

  $L_D \uparrow$ $Q \uparrow$ → locking range decreases

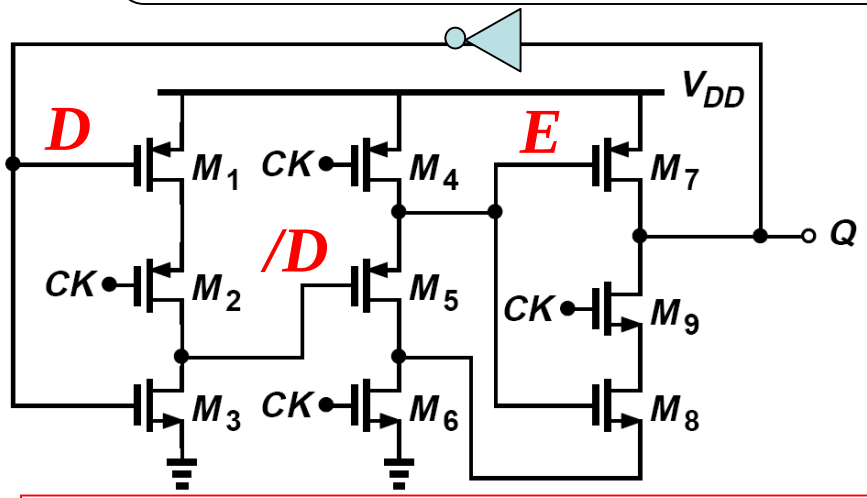
# True Single-Phase Clocking



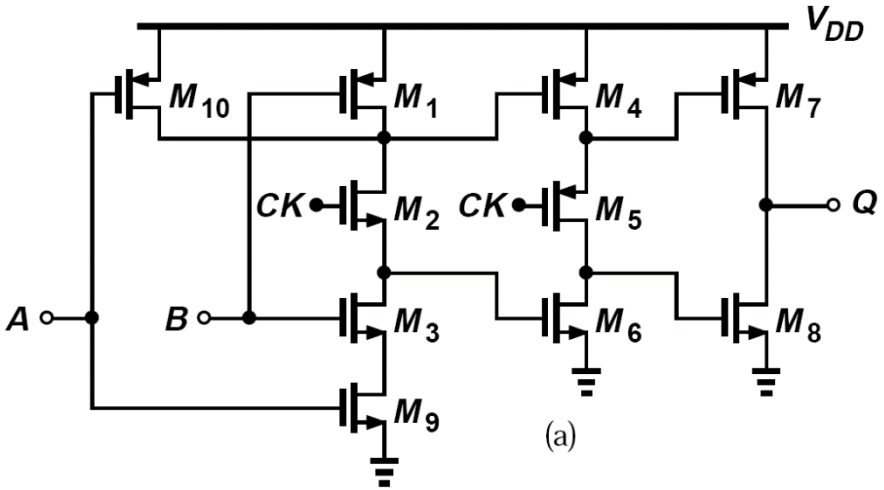

- When *CK* is high, the first stage operates as an inverter, impressing $\overline{D}$ at *A* and *E*. When *CK* goes low, the first stage is disabled and the second stage becomes transparent, writing $\overline{A}$ at *B* and *C* and hence making *Q* equal to *A*. The logical high at *E* and the logical low at *B* are degraded but the levels at *A* and *C* ensure proper operation of the circuit.

# TSPC Divide-by-2 Circuit and DFF with a NAND gate




Break the feedback, input=D
CK=low, E=high, M7&M9 off, Q holds
CK=high, D=low, /D=high, M6&M8&M9 on, Q=D=low
CK=high, D=high, /D=low, M5&M6 on, E=low,
M7 on, M8 off, Q=D=high

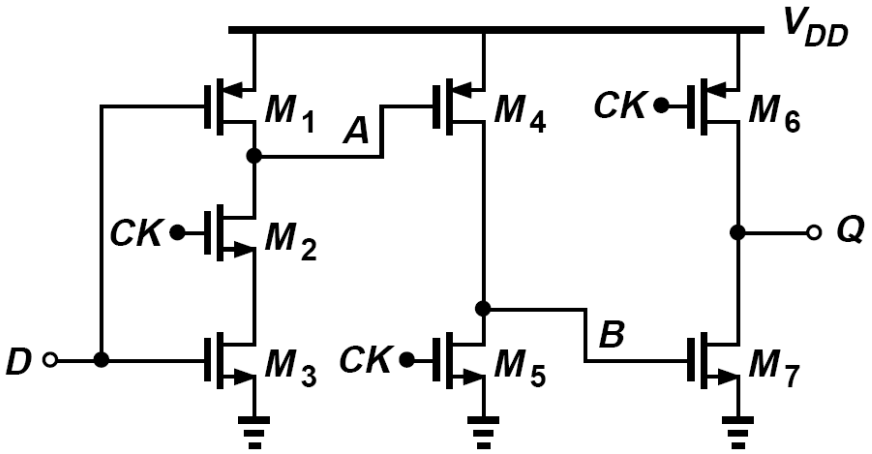
- This topology achieves relatively high speeds with low power dissipation, but, unlike CML dividers, it requires rail-to-rail clock swings for proper operation.
- The circuit consumes no static power and as a dynamic logic topology, the divider fails at very low clock frequencies due to the leakage of the transistors.

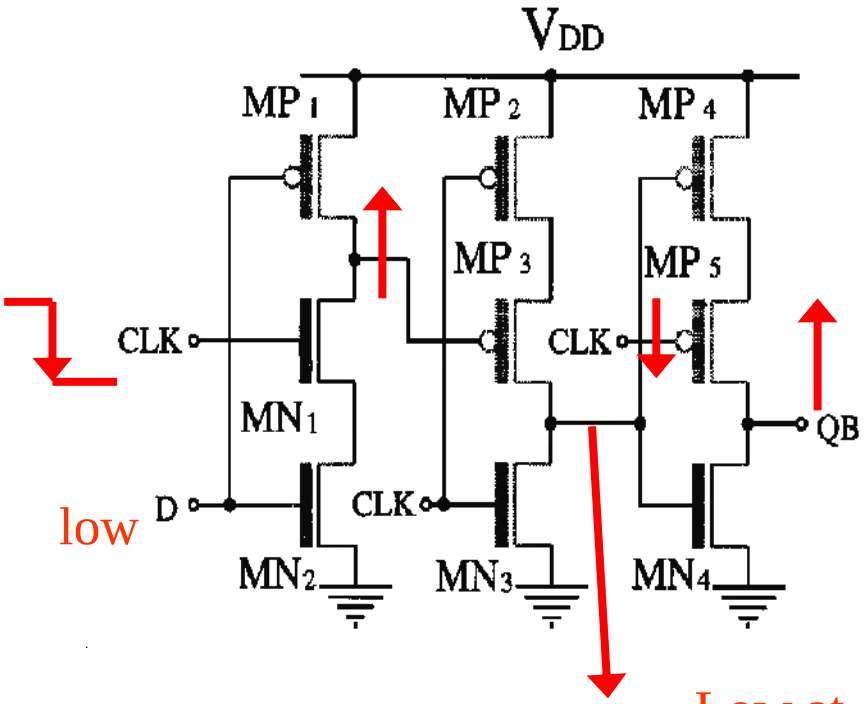



(a)

- A NAND gate can be merged with the master latch.
- In the design of TSPC circuit, one observes that wider clocked devices raises the maximum speed, but at the cost of loading the preceding stage.

# TSPC Using Ratioed Logic



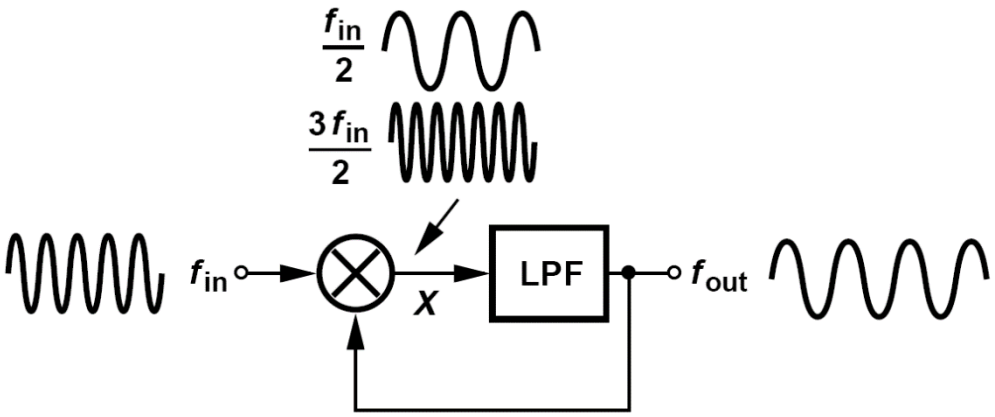



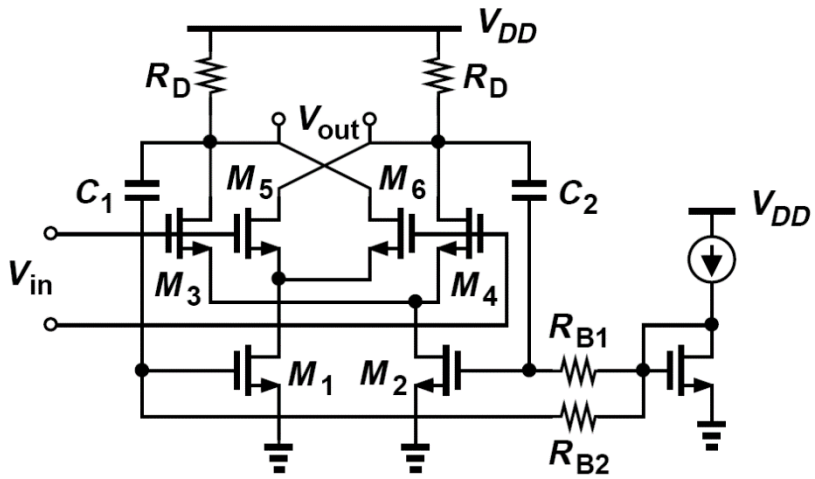

- **The slave latch is designed as "ratioed" logic, achieving higher speeds.**

IEEE JSSC, SC-31, pp. 749-, May 1996.

IEEE JSSC, SC-24, pp. 62-, Feb. 1989.

# Miller Divider

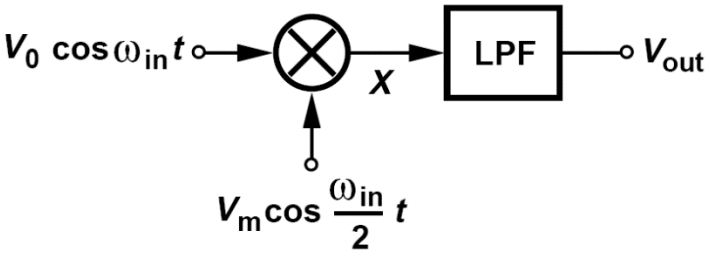


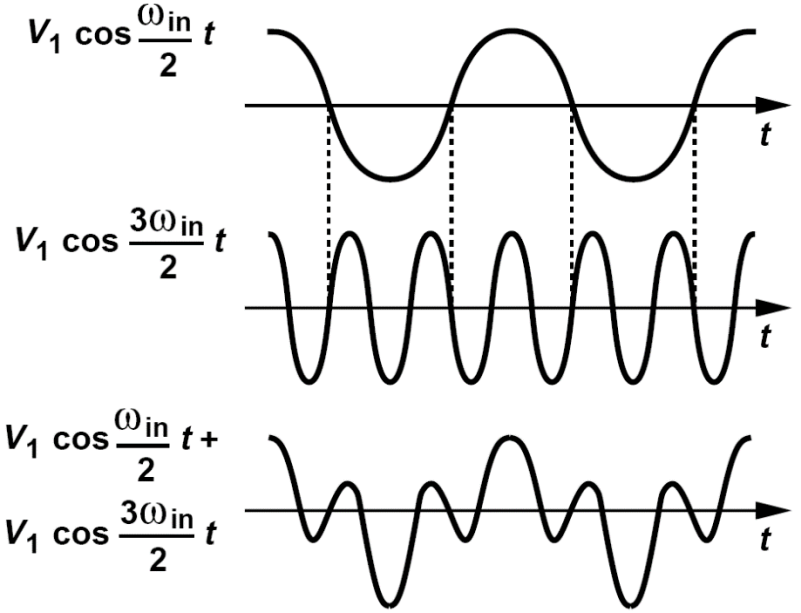




$$\cos(\alpha)\cos(\beta) = \cos(\alpha+\beta) + \cos(\alpha-\beta)$$

- If the required speed exceeds that provided by CML circuits, one can consider the "Miller divider", also known as the "dynamic divider"
- The Miller divider can achieve high speeds for two reasons: (1) the low-pass behavior can simply be due to the intrinsic time constant at the output node of the mixer and (2) the circuit does not rely on latching and hence fails more gradually than flipflops as the input frequency increases

# Why the Component at $3f_{in}/2$ Must be Sufficiently Small?



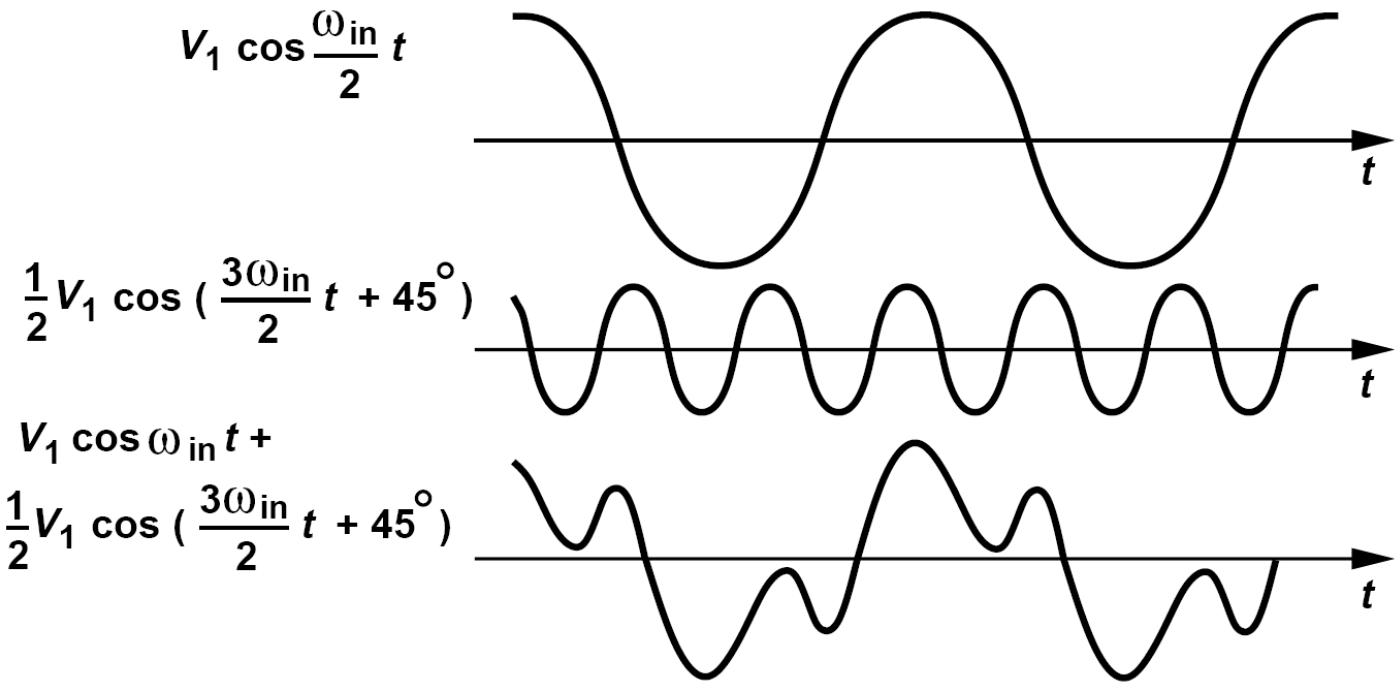




$$\begin{aligned} V_X(t) &= \alpha(V_0 \cos \omega_{in} t)\left(V_m \cos \frac{\omega_{in} t}{2}\right) \\ &= \frac{\alpha V_0 V_m}{2}\left(\cos \frac{\omega_{in} t}{2} + \cos \frac{3\omega_{in} t}{2}\right) \end{aligned}$$

- **This sum exhibits additional zero crossings, prohibiting frequency division if traveling through the LPF unchanged.**

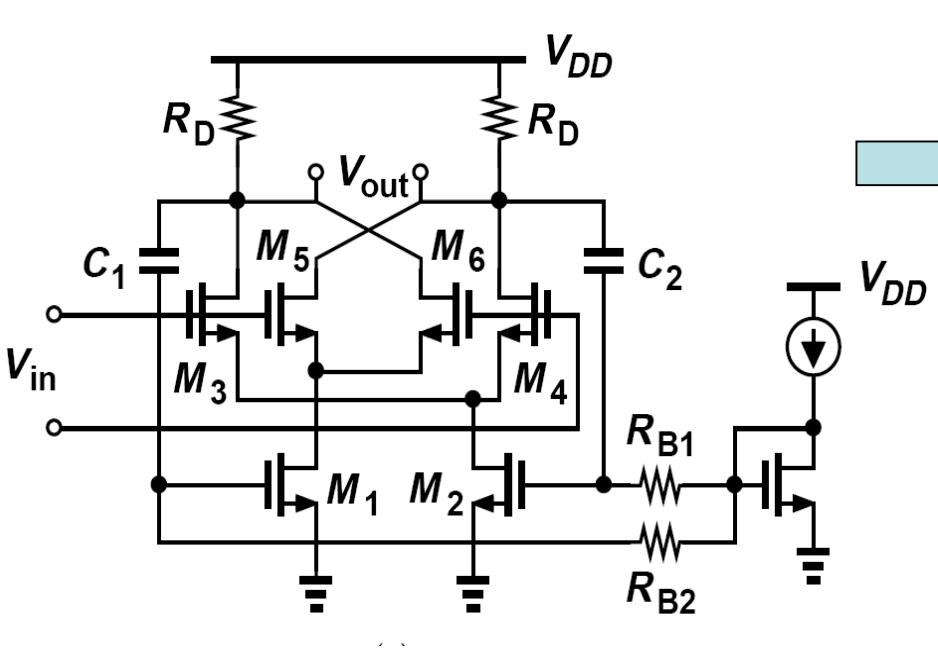
$$\cos(\alpha)\cos(\beta) = \cos(\alpha+\beta) + \cos(\alpha-\beta)$$

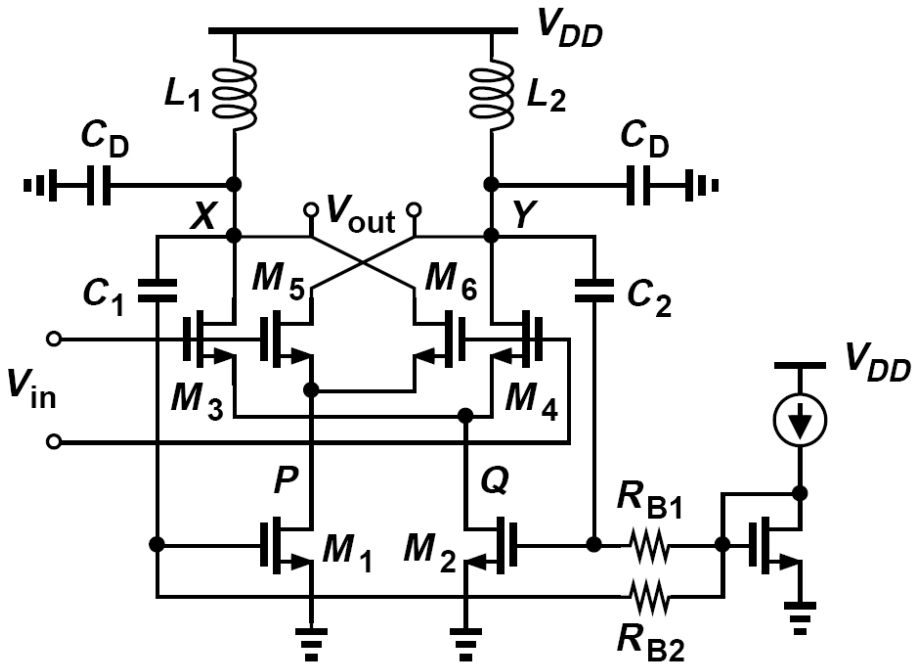
# Introducing Phase Shift in Miller Divider




- **The Miller divider operates properly if the third harmonic is attenuated and shifted so as to avoid the additional zero crossings.**

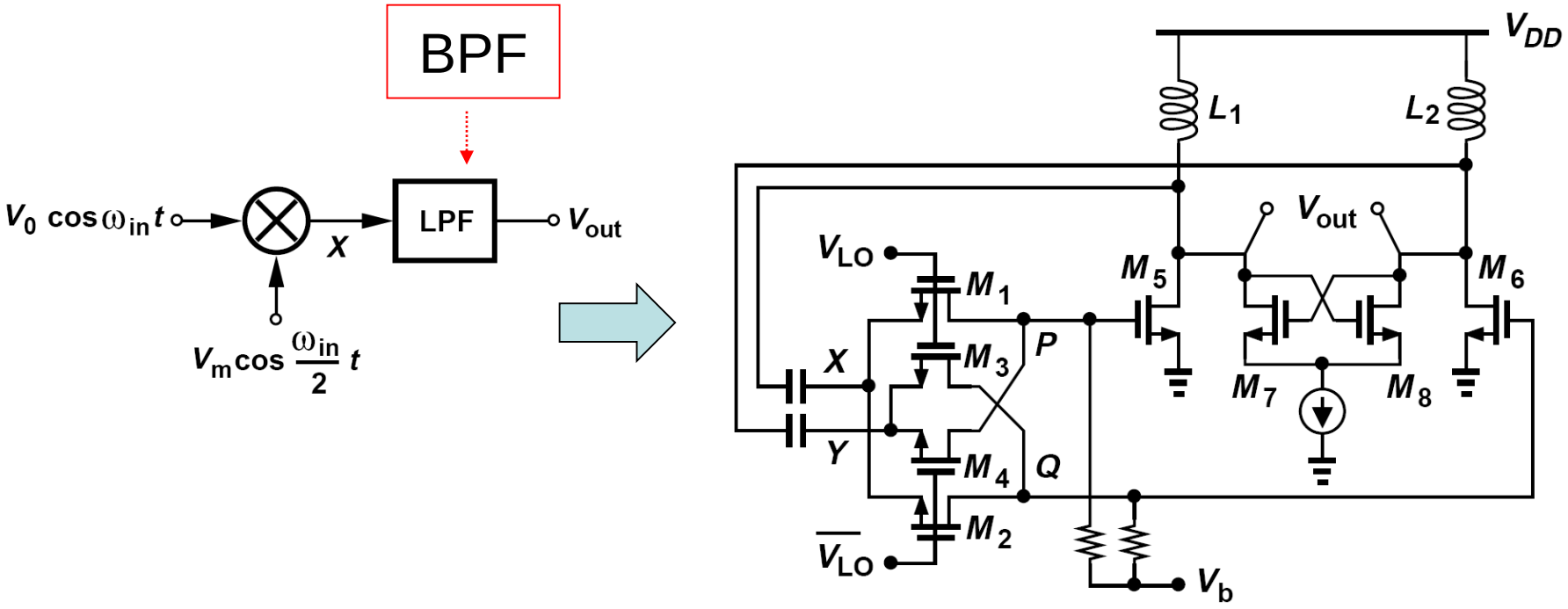
# Miller Divider with Inductive Load



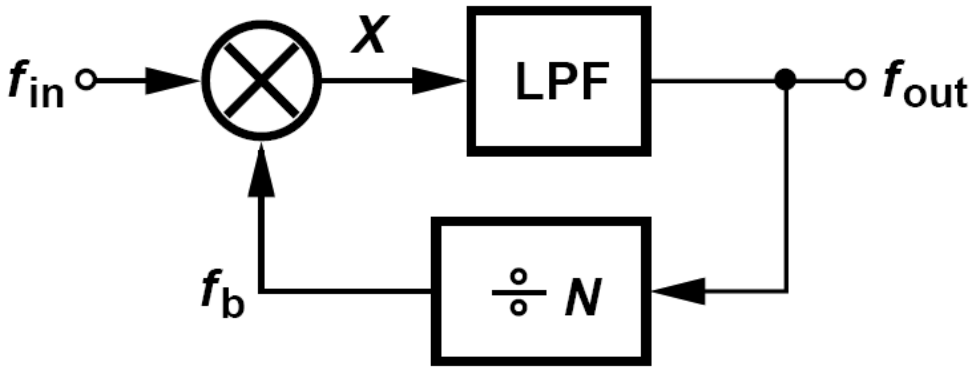

- **The tanks suppress the third-order harmonics**

# Miller Divider with Passive Mixers




- **Since the output CM level is near $V_{DD}$, the feedback path incorporates capacitive coupling, allowing the sources and drains of $M_1$-$M_4$ to remain about 0.4V above the ground. The cross-coupled pair $M_7$-$M_8$ can be added to increase the gain by virtue of its negative resistance.**

# Miller Divider with Other Moduli

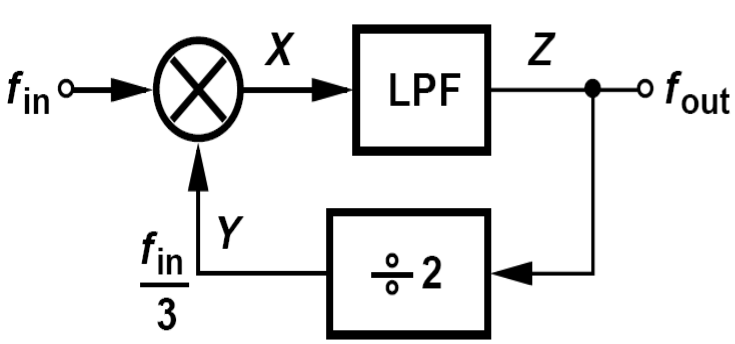


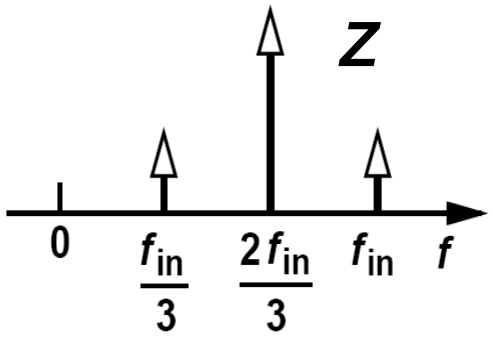

**A ÷*N* circuit in the feedback path creates $f_b = f_{out}/N$, yielding $f_{in} \pm f_{out}/N$ at *X*. If the sum is suppressed by the LPF, then $f_{out} = f_{in} - f_{out}/N$ and hence**

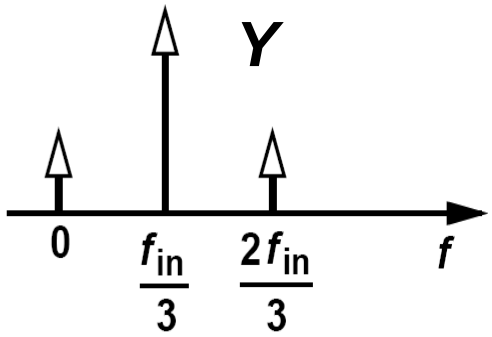
$$f_{out} = \frac{N}{N+1} f_{in} \qquad f_b = \frac{1}{N+1} f_{in}$$

- **The sum component at *X* comes closer to the difference component as *N* increases, dictating a sharper LPF roll-off.**
- **Another critical issue relates to the port-to-port feedthroughs of the mixer**

# Example : Effect of Feedthrough



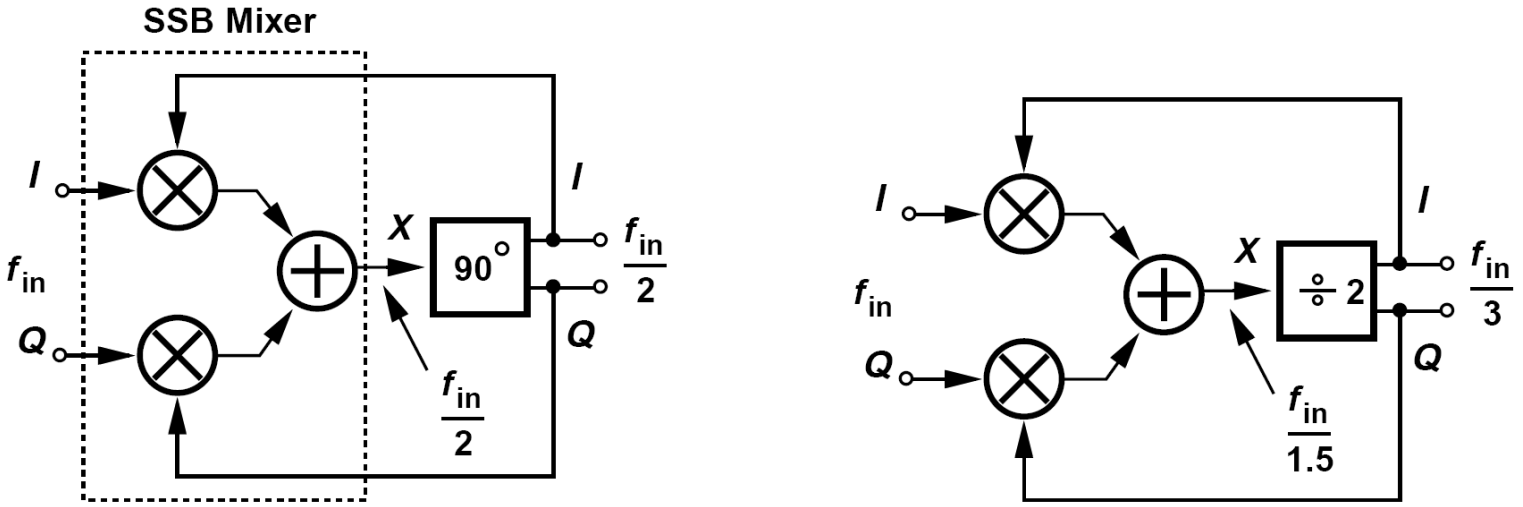




**Assume *N* = 2 . The feedthrough from the main input to node *X* produces a spur at $f_{in}$. Similarly, the feedthrough from *Y* to *X* creates a component at $f_{in}/3$. The output therefore contains two spurs around the desired frequency. The additional zero crossing will result in a malfunction.**

$$f_{in} - \frac{f_{out}}{2} = f_{out} \Rightarrow f_{out} = \frac{2f_{in}}{3}$$

**The spectrum at Y : Example 9.12**

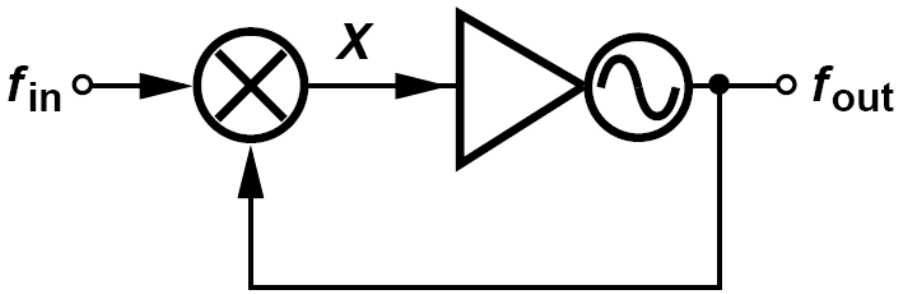
# Miller Divider Using SSB Mixer



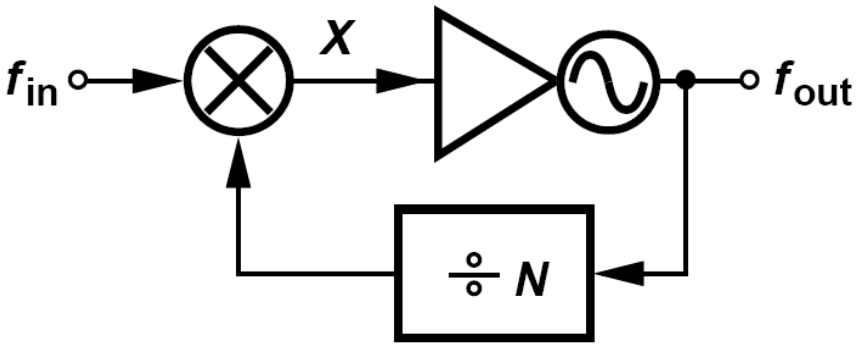

$$\cos(\alpha)\cos(\beta) \mp \sin(\alpha)\sin(\beta) = \cos(\alpha \pm \beta)$$

- **The Miller divider frequency range can be extended through the use of a single-sideband (SSB) mixer. It suppresses the sum component by SSB mixing rather than filtering to avoid the additional zero crossing.**
- **The use of SSB mixing prove useful if the loop contains a divider that generates quadrature outputs. Topology in (b) achieves a wide frequency range and generates quadrature outputs. But it requires quadrature LO phases.**

# Injection-Locked Dividers (ILDs)




- Based on oscillators that are injection-locked to a harmonic of their oscillation frequency
- If $f_{in}$ varies across a certain "lock range", the oscillator remains injection-locked to the $f_{in}$-$f_{out}$ component at node *X*




The mixer yields two components at node *X*, namely, $f_{in} - f_{out}/N$ and $f_{in} + f_{out}/N$. If the oscillator locks to the former, then $f_{in} - f_{out}/N = f_{out}$ and hence

$$f_{out} = \frac{N}{N+1} f_{in}$$

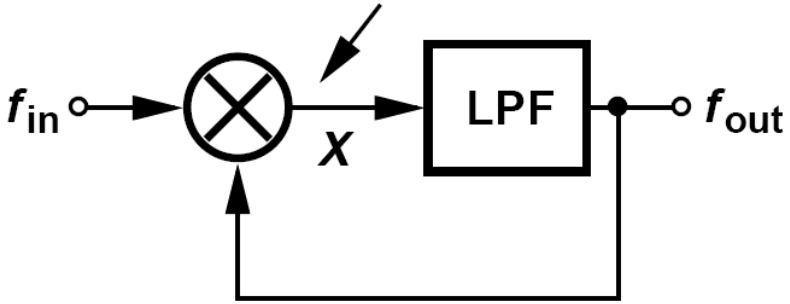
The oscillator lock range must therefore be narrow enough to lock to only one of the two components.

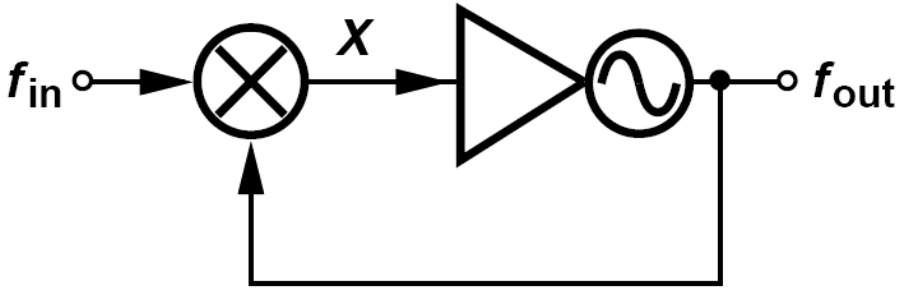
Similarly, if the oscillator locks to the latter then

$$f_{out} = \frac{N}{N-1} f_{in}$$

# Miller Divider and Injection-Locked Divider

**What is the difference between Miller divider and ILD?**
**The ILD oscillates even input amplitude is zero, but Miller divider does not. Generally, ILD has a narrower operation range than Miller divider.**

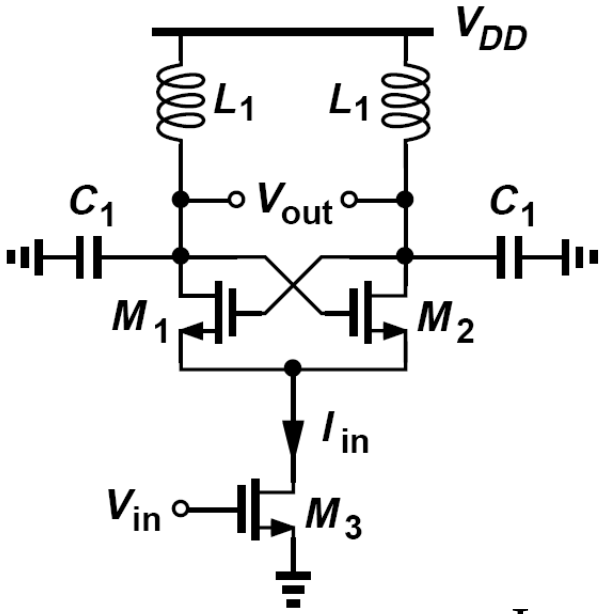


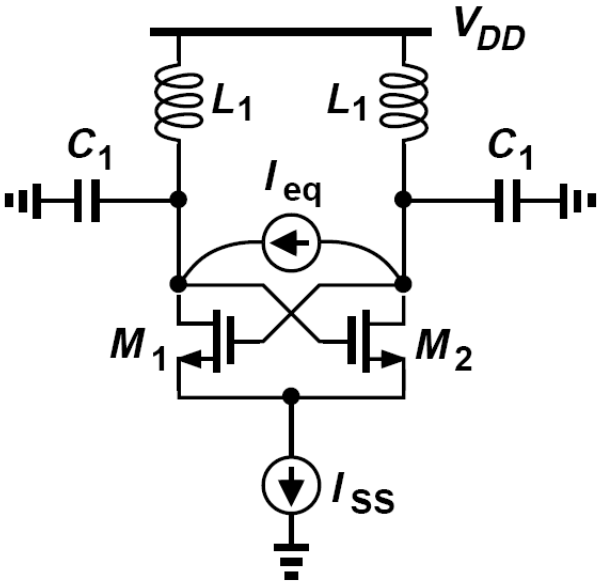




IEEE JSSC, pp. 2109-, Aug. 2019

IEEE JSSC, pp. 2122-, Aug. 2019

# Implementation of ILD



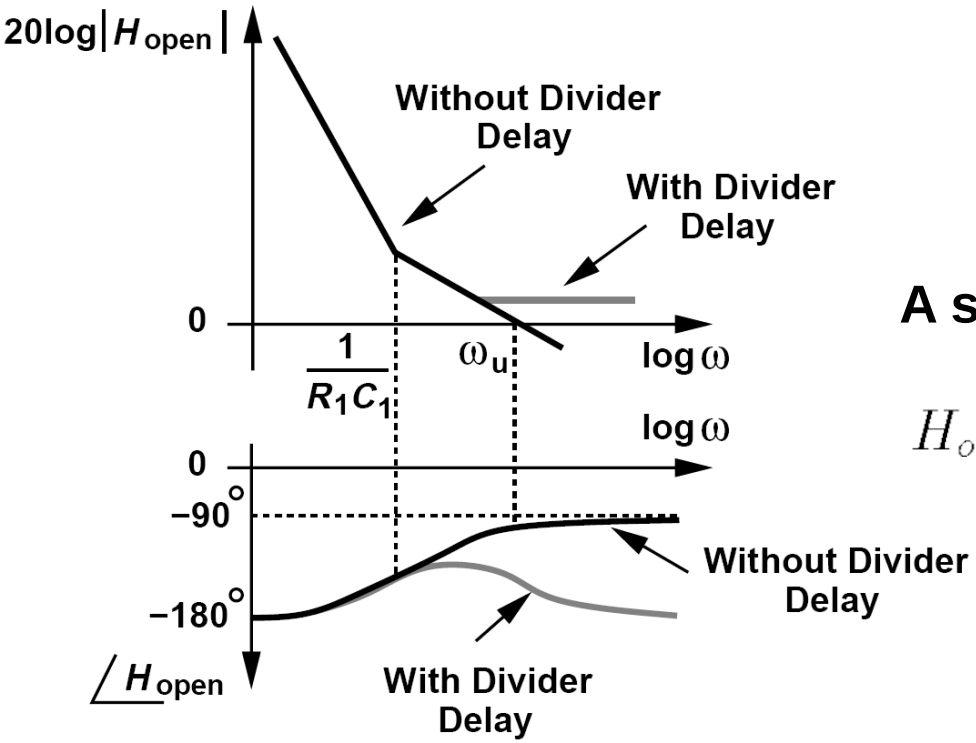

[18] $\Delta\omega_{out,two-side} = \frac{\omega_0}{Q} \times \frac{I_{inj}}{I_{SS}} = \frac{\omega_0}{Q} \times \frac{I_{inj}}{I_{osc}}$ $\qquad I_{inj} = \frac{2}{\pi} \times I_{in}$ Page 371

**The output frequency range across which the circuit remains locked is given by**

$$\Delta\omega_{out} = \frac{\omega_0}{Q}\left(\frac{2}{\pi}\frac{I_{in}}{I_{osc}}\right)$$

**The input lock range is twice this value:** $\Delta\omega_{in} = \frac{\omega_0}{Q}\left(\frac{4}{\pi}\frac{I_{in}}{I_{osc}}\right)$

# Divider Delay and Phase Noise: Effect of Divider Delay




**A stage with a constant delay of $\Delta T$**

$$H_{open}(s) = \frac{I_P}{2\pi}\left(R_P + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{NS}e^{-\Delta T \cdot s}.$$

$$e^{-s\cdot\Delta T} \approx 1 - s\cdot\Delta T \quad if \left|s\cdot\Delta T\right| << 1$$

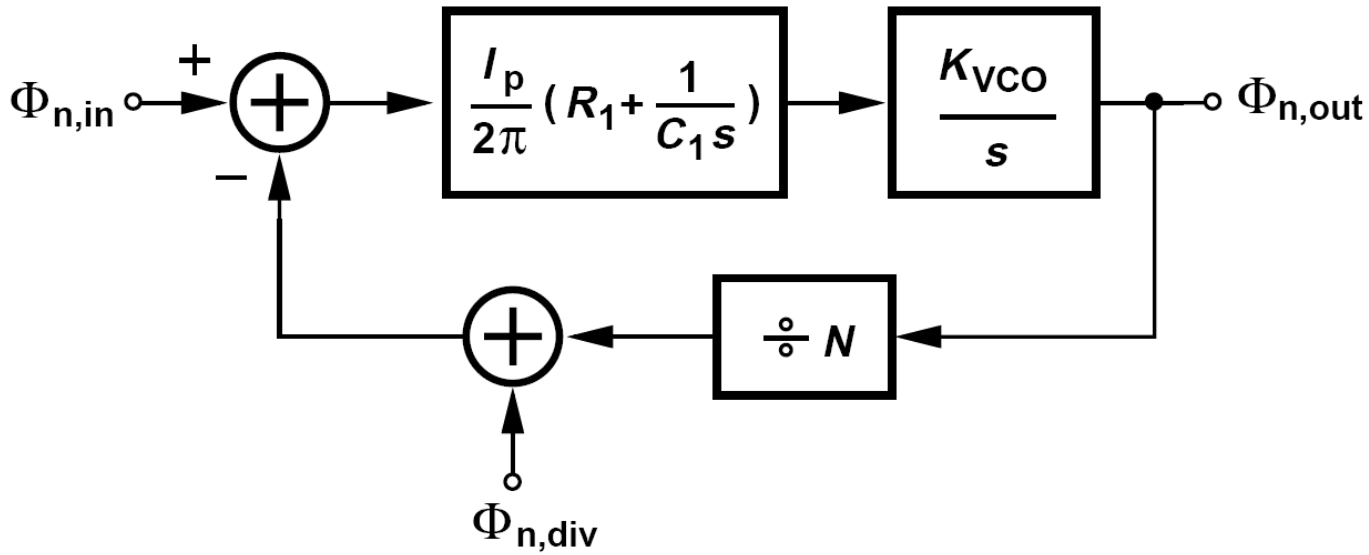
- **The zero has two undesirable effects: it flattens the gain, pushing the gain crossover frequency to higher values (in principle, infinity), and it bends the phase profile downward.**

**This zero must remain well above the original unity-gain bandwidth of the loop:**

$$\frac{1}{\Delta T} \approx 5\omega_u$$

$$\omega_u^2 = \left(2\zeta^2 + \sqrt{4\zeta^4 + 1}\right)\omega_n^2. \qquad (9.67)$$

# Effect of Divider Phase Noise

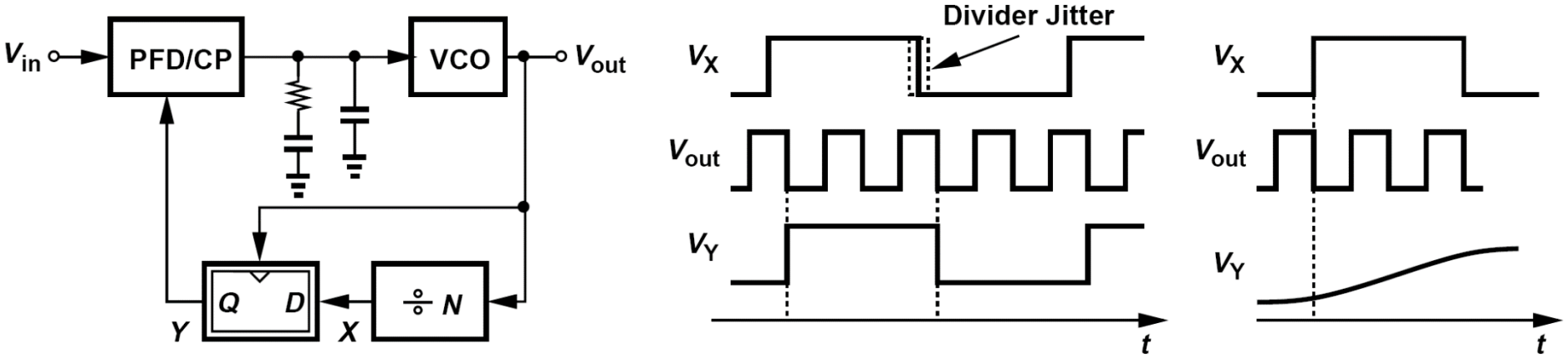



- **The output phase noise of the divider directly adds to the input phase noise, experiencing the same low-pass response as it propagates to $\phi_{out}$. In other words, $\phi_{n,div}$ is also multiplied by a factor of N within the loop bandwidth.**

**For the divider to contribute negligible phase noise, we must have**

$$\phi_{n,div} \ll \phi_{n,in}$$

# Use of Retiming FF to Remove Divider Phase Noise



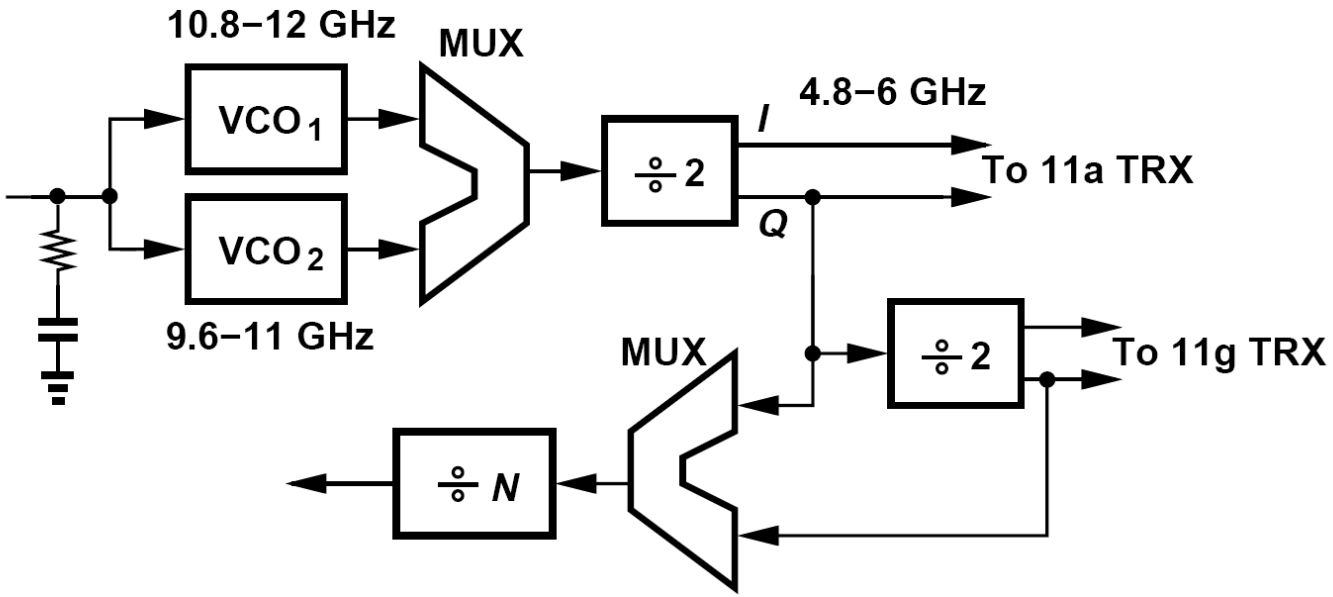

- **If the divider phase noise is significant, a retiming flipflop can be used to suppress its effect.**
- **In essence, the retiming operation bypasses the phase noise accumulated in the divider chain.**
- **“Metastable“ problem occurs, if a VCO edge is close to the transition at node Vx.**

IEEE T-CAS-II, pp. 200-, April 2011

# Synthesizer Design: Section 13.4

**We want to design an integer-N synthesizer with a reference of 20MHz for 11a (5.1~5.9GHz) and 11g (2.4~2.48GHz) bands.**

**A VCO of 2.4GHz and A VCO of 5-6GHz with the phase noise of -101dBc/Hz at an offset frequency of 1MHz. The $VCO_2$ from 10.8 GHz to 12 GHz has the phase noise of -101+6=-95dBc/Hz.**



# VCO Design (I)---Preliminary 12 GHz VCO

**We choose the tuning range of the VCOs as follows. One VCO, $VCO_1$, operates from 9.6 GHz to 11 GHz, and the other, $VCO_2$, from 10.8 GHz to 12 GHz. We begin with $VCO_2$**

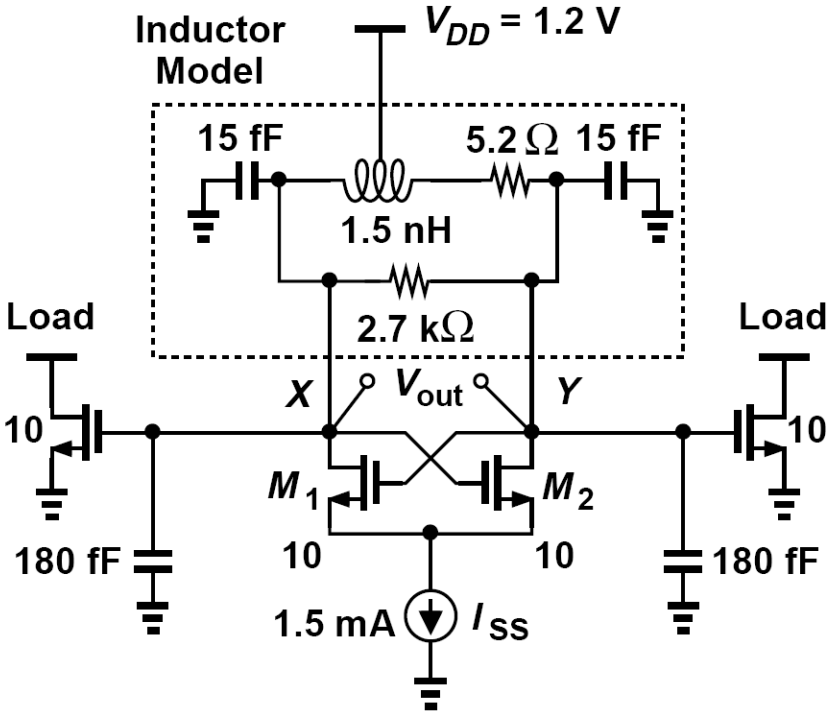
$$f_o = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.75\text{nF} * (180 + 15)\text{fF}}}$$

$$= 13\text{GHz}$$

$$R_p = Q\omega_o L = 10 \cdot 2\pi \cdot 13\text{GHz} \cdot 0.75\text{nF}$$

$$= 613\Omega$$

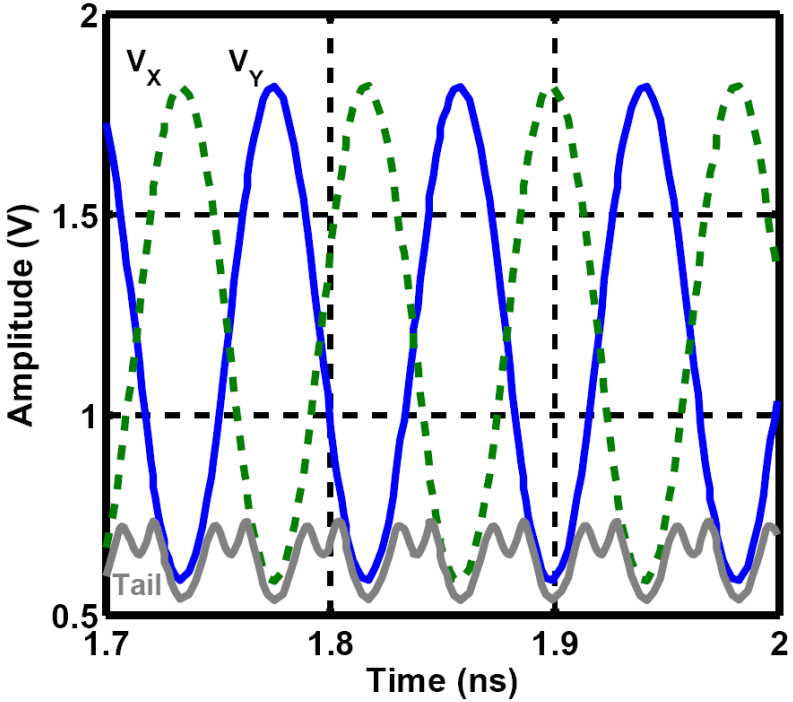
$$V_{pp} = \frac{4}{\pi} R_P I_{SS} = 1.17\text{V}$$

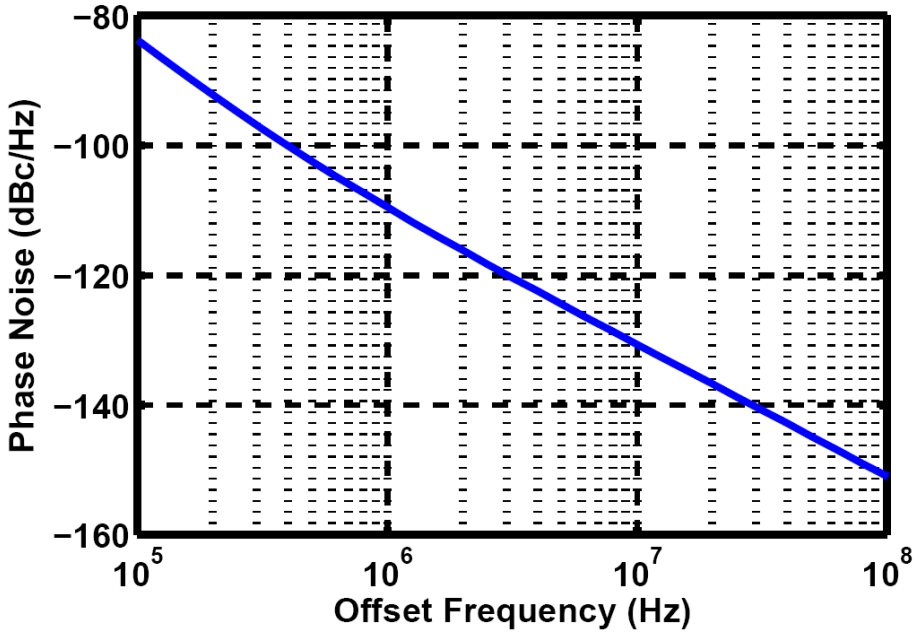



- **Assume a single-ended load inductance of 0.75 nH, *Q* = 10. Yielding a single-ended peak-to-peak output swing of 1.2 V. We choose a width of 10 *μ*m for cross-coupled transistors. Finally we add enough constant capacitance to obtain an oscillation frequency of about 12 GHz.**

# VCO Design (II)---Simulation Result of Preliminary Design

**We wish to briefly simulate the performance of the circuit before adding the tuning devices.**



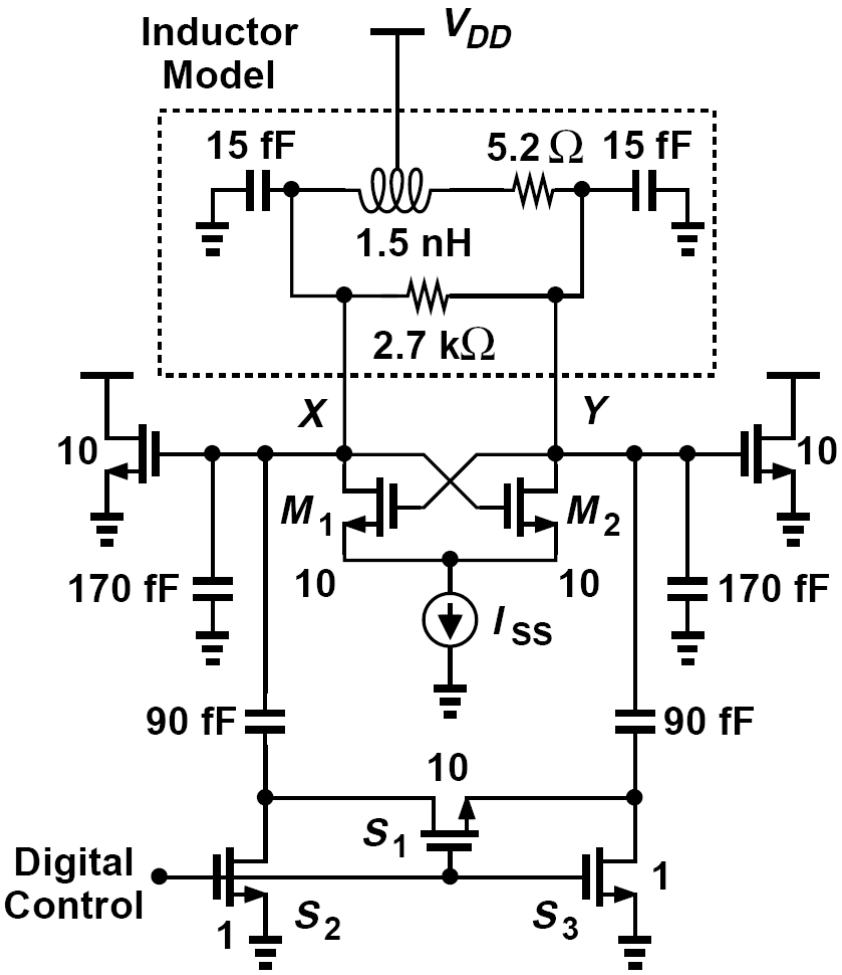




- **Simulations suggest a single-ended peak-to-peak swing of about 1.2 V. Also, the phase noise at 1-MHz offset is around -109 dBc/Hz, well below the required value. The design is thus far promising.**
- **However, the phase noise is sensitive to the tail capacitance. (CH8, p. 556)**

# VCO Design (III)---Add Capacitance for Tuning

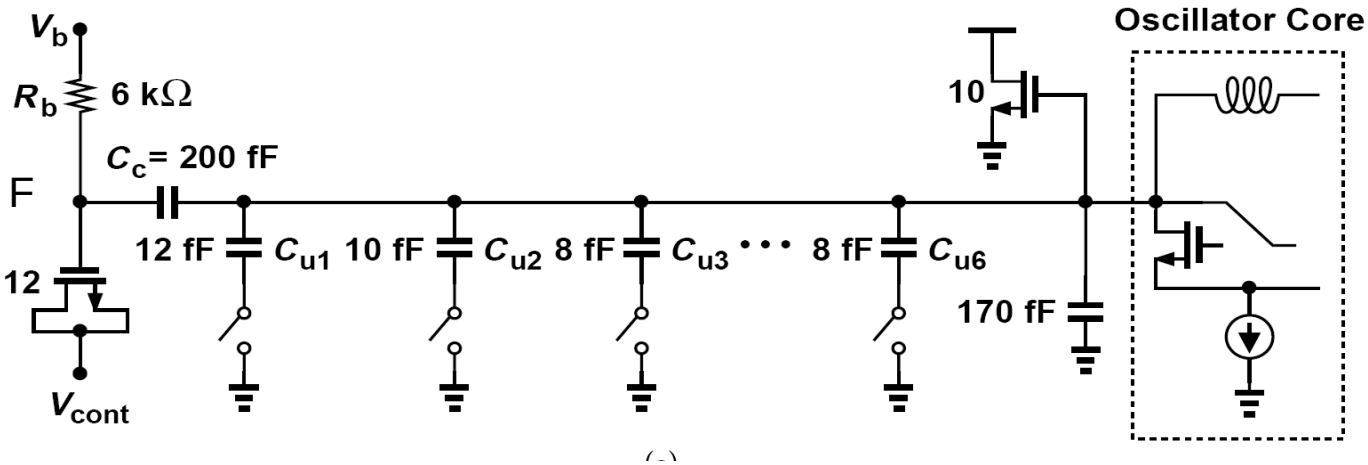
**Now, we add a switched capacitance of 90 fF to each side so as to discretely tune the frequency from 12 GHz to 10.8 GHz.**

- **The size of the switches in series with the 90-fF capacitors must be chosen according to the trade-off between their parasitic capacitance in the off state and their channel resistance in the on state.**
- **The voltage swing decreases considerably if the on-resistance is not sufficiently small.**
- **Simulations indicate that the frequency can be tuned from 12.4 GHz to 10.8 GHz but the single-ended swings fall to about 0.8 V at the lower end. To remedy the situation, we raise the tail current to 2mA.**

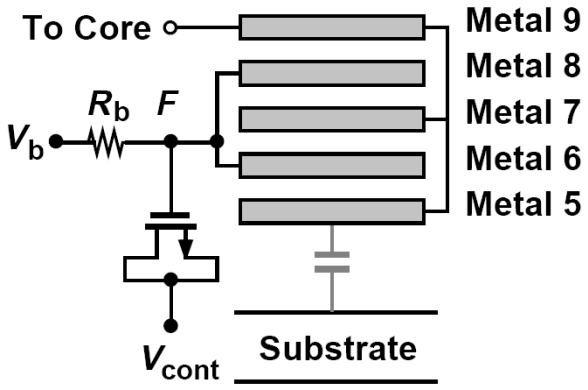


# VCO Design (IV)---Add Varactors

**In the next step, we add varactors to the VCO and decompose the switched capacitors into smaller units, thus creating a set of discretely-spaced continuous tuning curves with some overlap.**

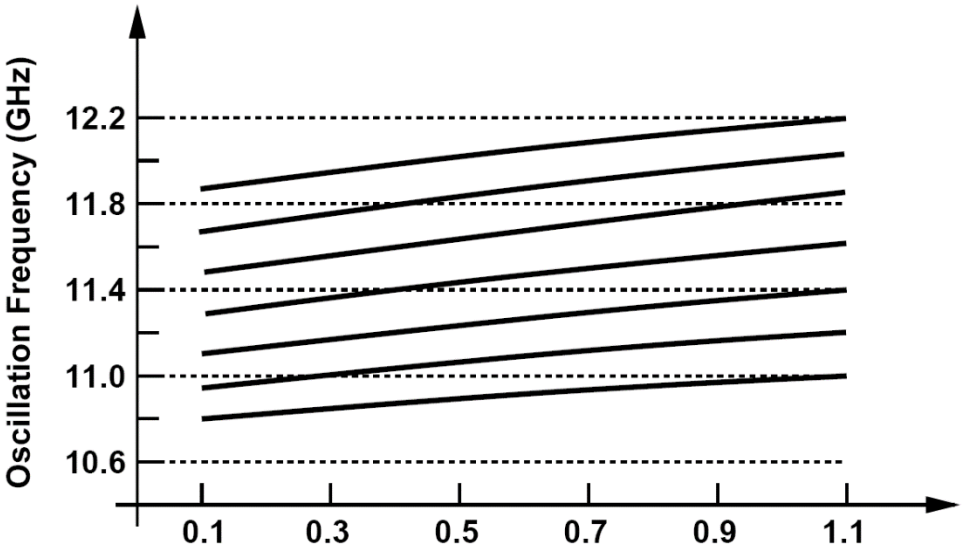


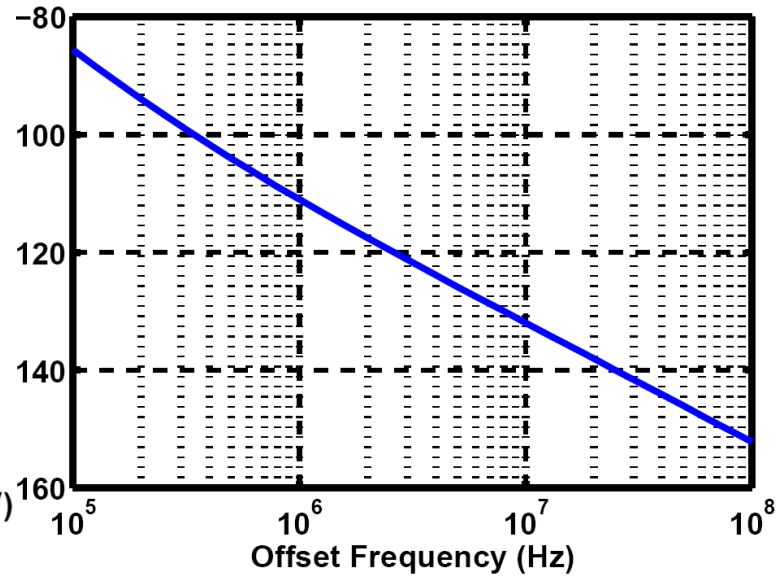

- **It demands some iteration in the choice of the varactors' size and the number and values of the unit capacitors.**
- **We still have floating switches even though they are not shown.**
- **To obtain a wide continuous tuning range, the gate of the varactor is capacitively coupled to the core and biased at $V_b \approx 0.6$ V.**



# VCO Design (V)---Tuning Characteristics and Phase Noise

**Figure below shows VCO's tuning characteristics obtained from simulations and phase noise with all of the capacitors switched into the tank.**

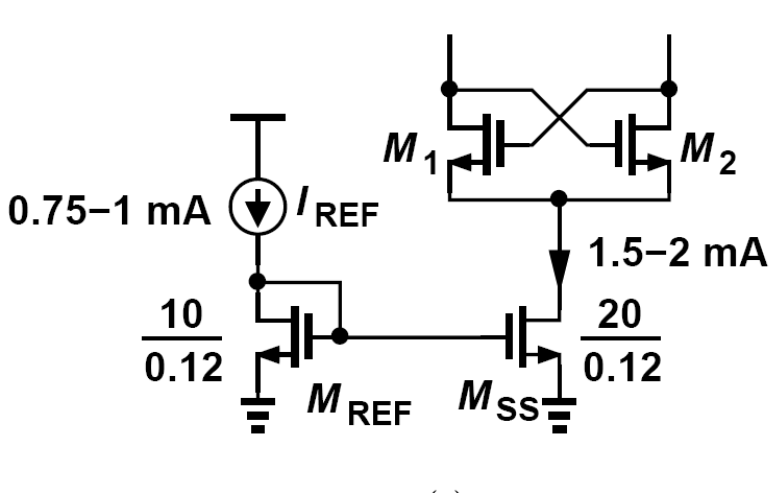


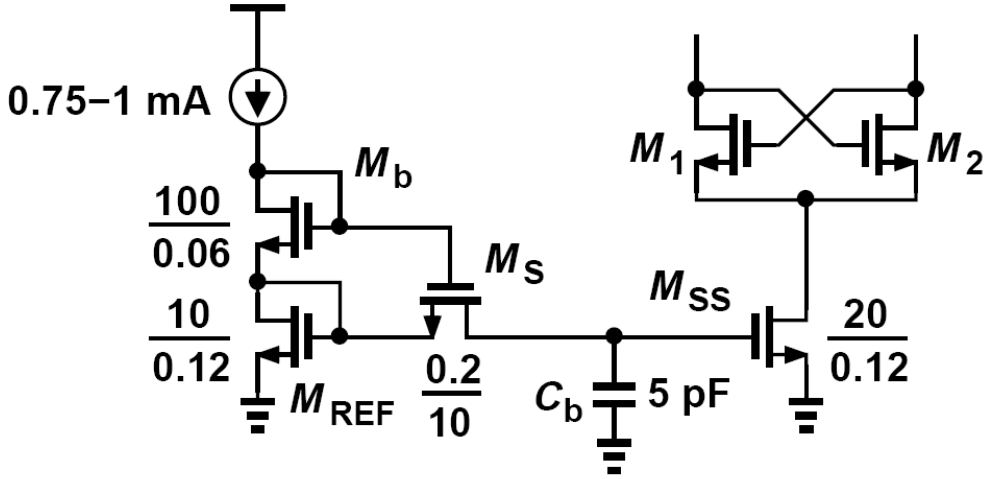




- **The control can operate properly across this range. We note that $K_{VCO}$ varies from about 200 MHz/V to 300 MHz/V.**

# VCO Design (VI)---Replace Ideal Tail Current with Current Mirror

**In the last step of our VCO design, we replace the ideal tail current source with a current mirror.**

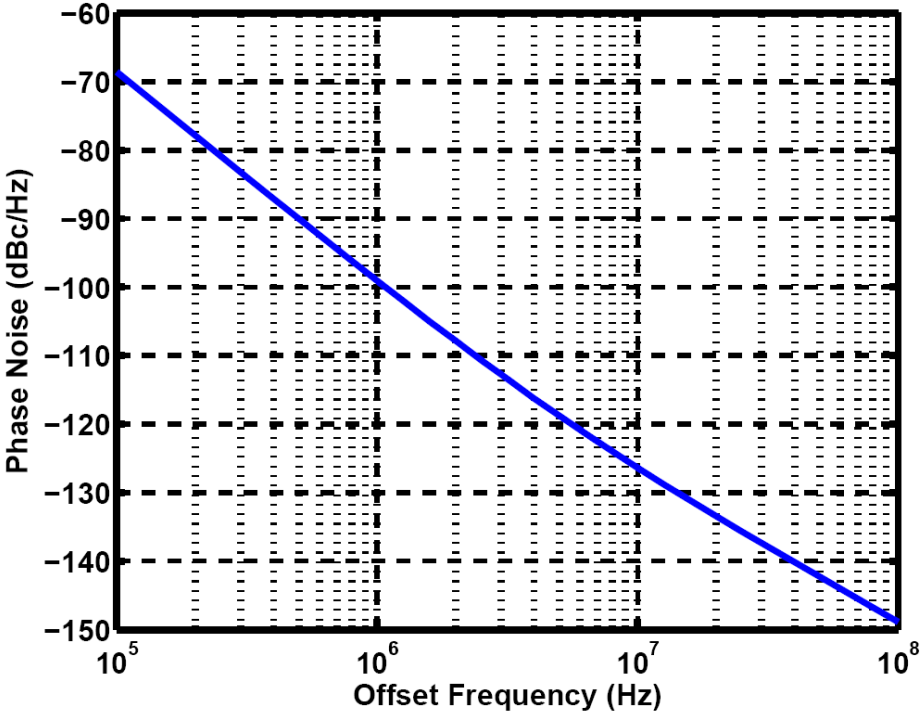


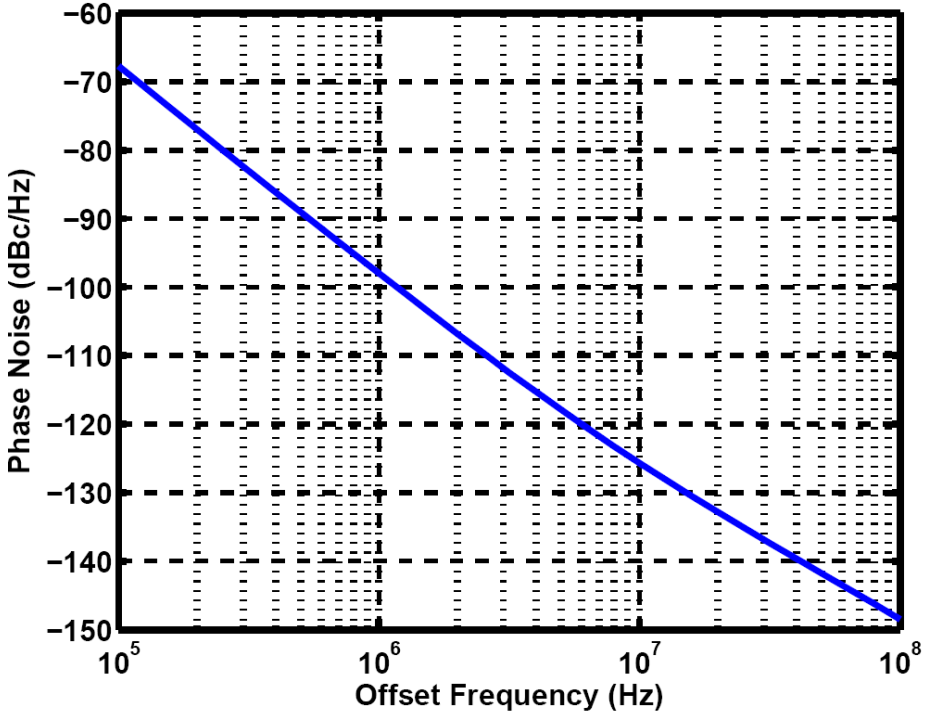




- **This arrangement incorporates a channel length of 0.12 $\mu$m to improve the matching between the two transistors in the presence of a $V_{DS}$ difference. The width of $M_{SS}$ is chosen so as to create a small overdrive voltage, allowing the $V_{GS}$ to be approximately equal to $V_{DS}$ (≈ 500 mV).**

# VCO Design (VII)---Raised Phase Noise

**The current mirror drastically raises the phase noise of the VCO, from -111 dBc/Hz to -100 dBc/Hz at 10.8 GHz and from-109 dBc/Hz to-98 dBc/Hz at 12.4 GHz (both at 1-MHz offset)**

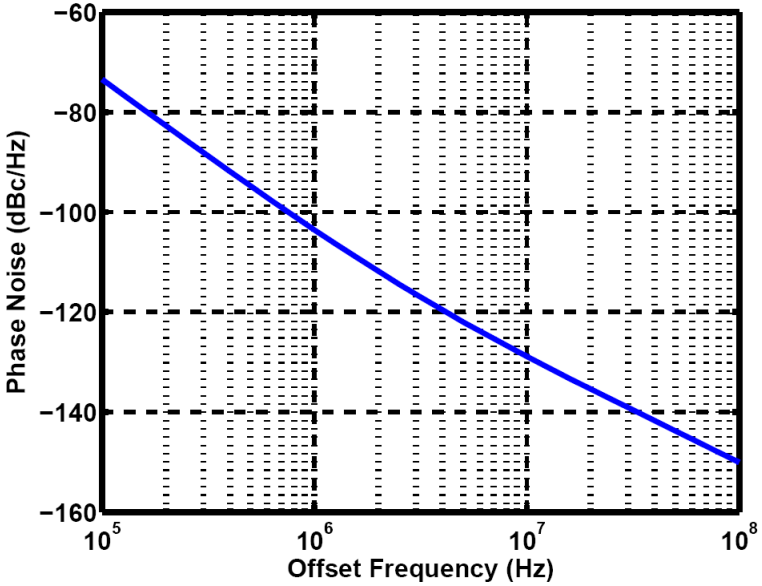


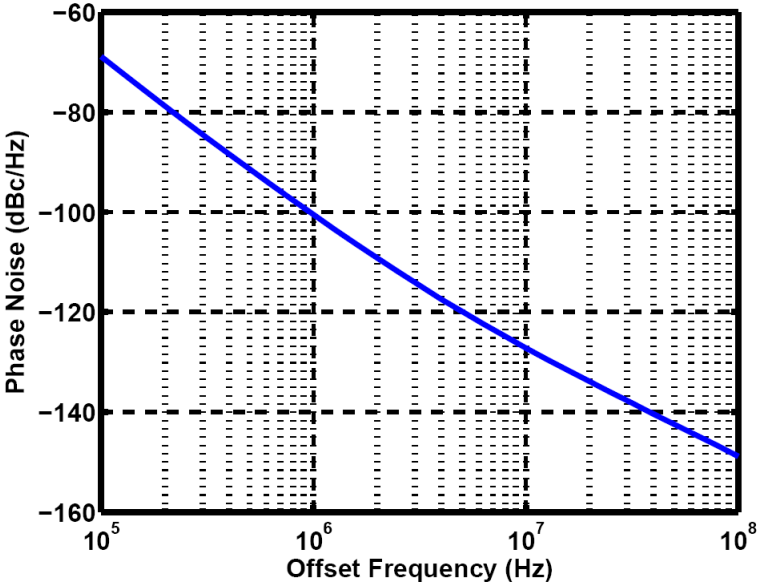




- **Most of the phase noise now arises from the thermal and flicker noise of $M_{REF}$ and $M_{SS.}$**

# VCO Design (VIII)---Modification to Suppress the Noise

**A simple modification can suppress the contribution of $M_{REF}$ . As shown above, we insert a low-pass filter between the two transistors, suppressing the noise of $M_{REF}$ (and $I_{REF}$ ).**




- **To obtain a corner frequency well below 1 MHz:**

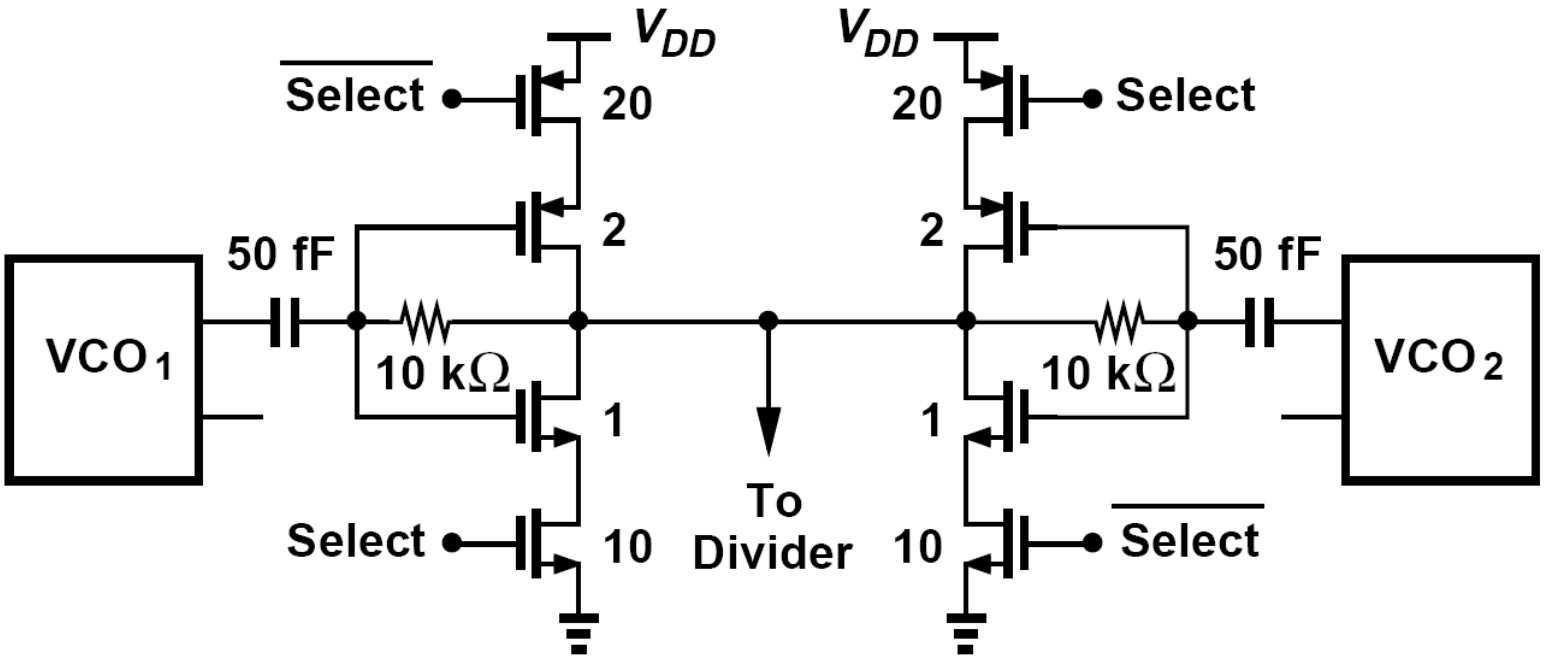
  **(1) bias MS with a small overdrive voltage, which is provided by the wide diode-connected transistor $M_b$;**

  **(2) select a width of 0.2 $\mu$m and a length of 10 $\mu$m for $M_S$;**

  **(3) choose a value of 5 pF for $C_b$.**

# Multiplexing Two VCOs

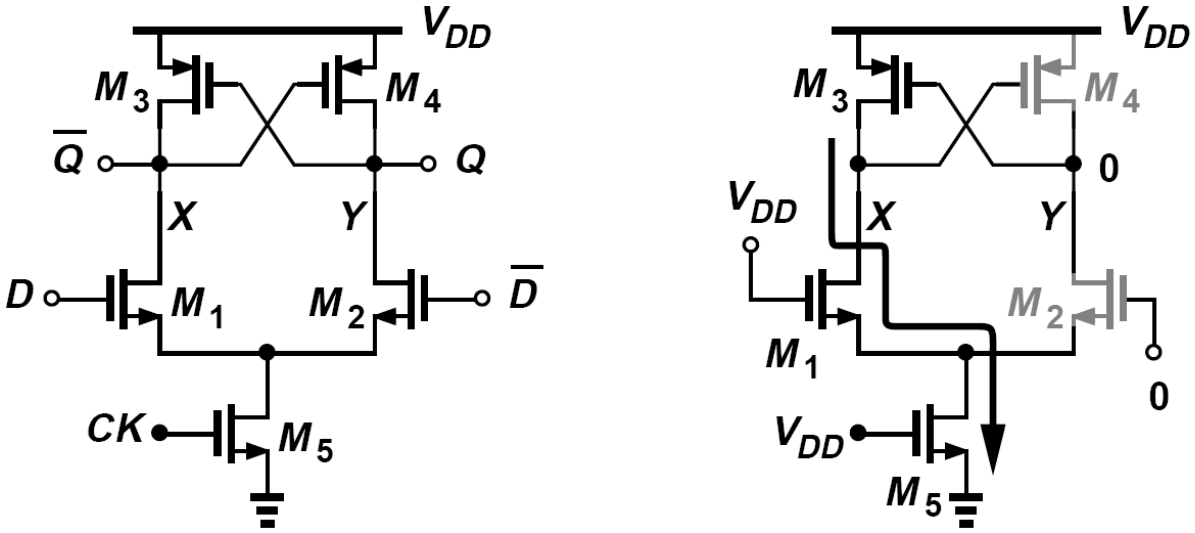
**The outputs of the two VCOs must be multiplexed. With rail-to-rail swings available, simple inverters can serve this purpose.**




- **Each inverter is sized according to an estimated fanout necessary to drive the subsequent divide-by-2 circuit.**
- **The VCO outputs have a CM level equal to $V_{DD}$ and are therefore capacitively coupled to the MUX.**

# Divider Design: Latch in a Divide-by-2 Circuit

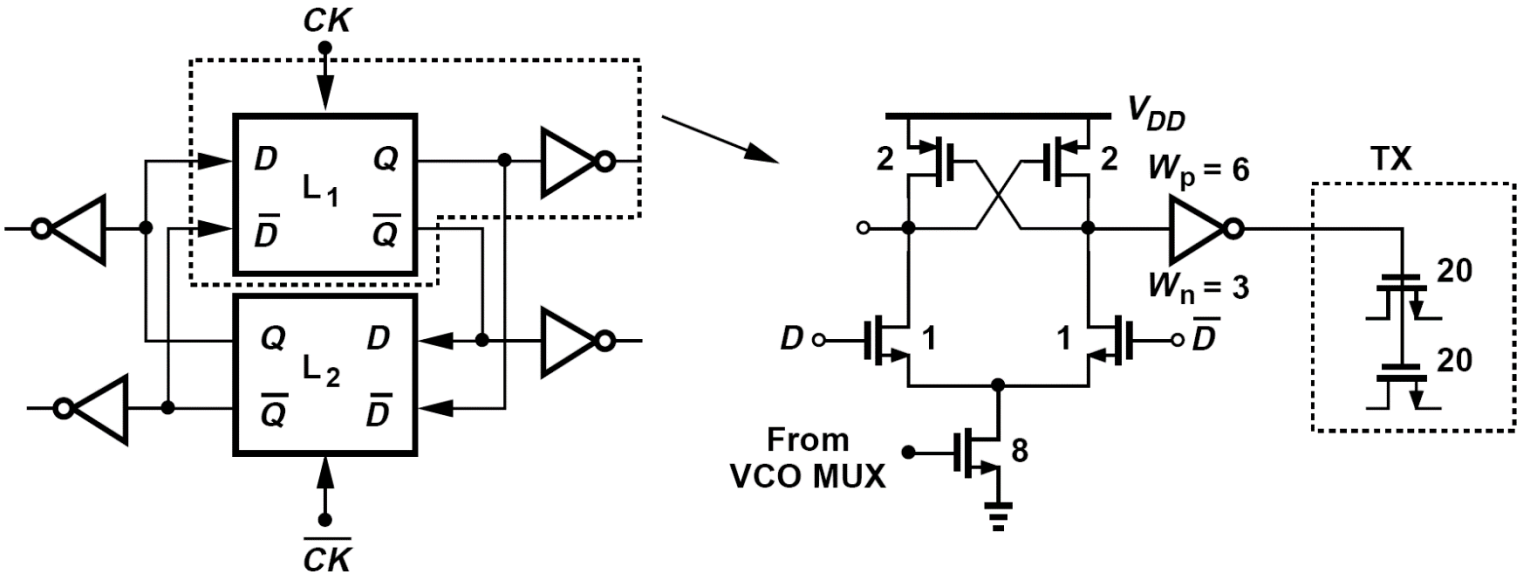
**The multiplexed VCO outputs must be divided by two so as to generate quadrature outputs. With rail-to-rail swings available at the MUX output, we seek a simple and efficient topology.**




- **This topology employs dynamic logic; leakage currents eventually destroy the stored state if *CK* is low for a long time.**
- **The latch is based on ratioed logic, requiring careful sizing.**

# Divide-by-2 Circuit: Driving a Large Load Capacitance

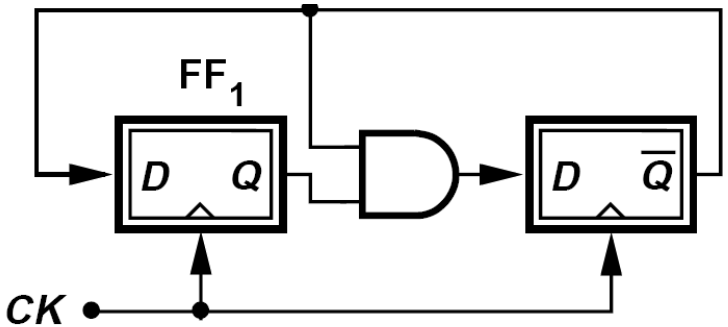
**As with other latches, the above circuit may fail if loaded by a large load capacitance. For this reason, we immediately follow each latch in the divide-by-2 circuit by inverters.**



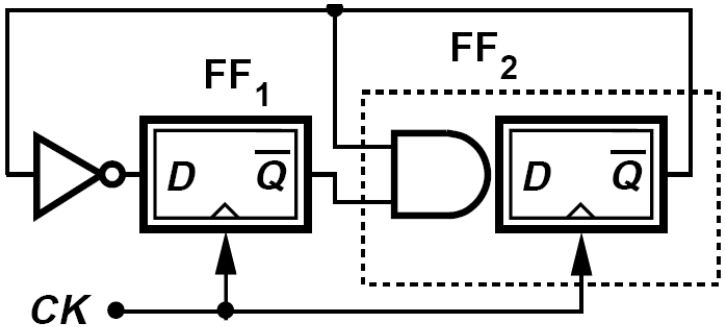

- **The inverters present a small load to the latch but must drive a large capacitance themselves, thereby producing slow edges.**
- **Frequency dividers typically demand a conservative design because:**
  **(1) the layout parasitics tend to lower the speed considerably**
  **(2) in the presence of process and temperature variations, the divider must handle the maximum frequency arriving from the VCO.**

# Dual-Modulus Divider

**The pulse-swallow counter necessary for the synthesizer requires a prescaler, which itself employs a dual-modulus divider. Such a divider must operate up to about 6.5 GHz.**

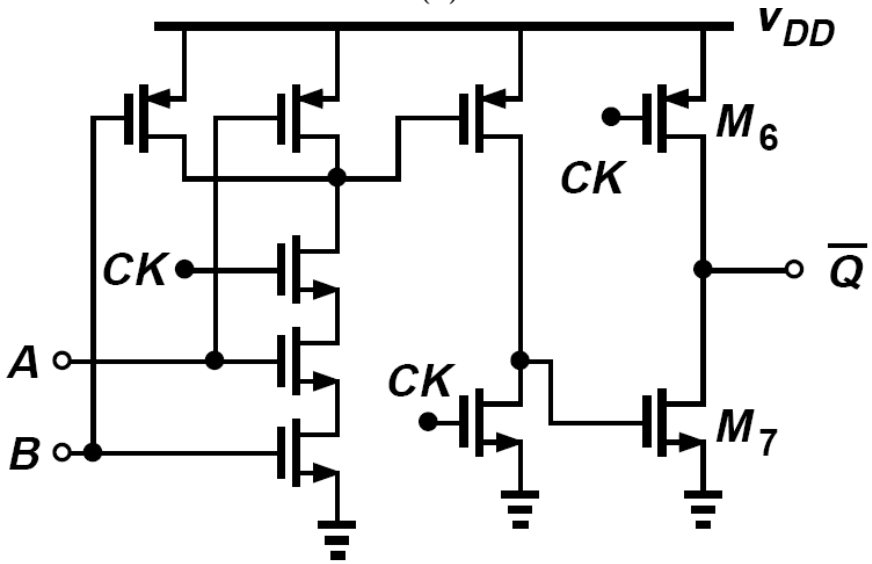



(a)




(b)

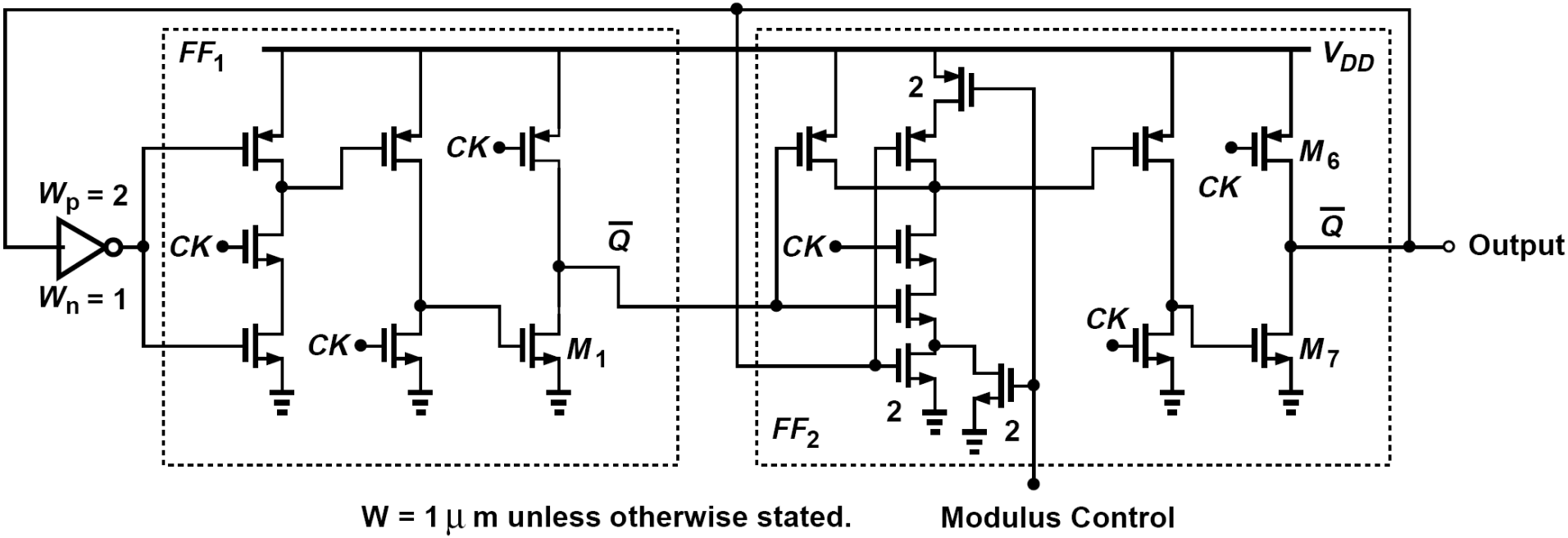
- **The Chang-Park-Kim flipflop shown in (a) provides only a Q output. We modify it to that shown in (b), where $FF_1$ is preceded by an inverter.**
- **We also wish to merge the AND gate with the second flipflop so as to improve the speed (c)**




(c)

# ÷3/4 Circuit

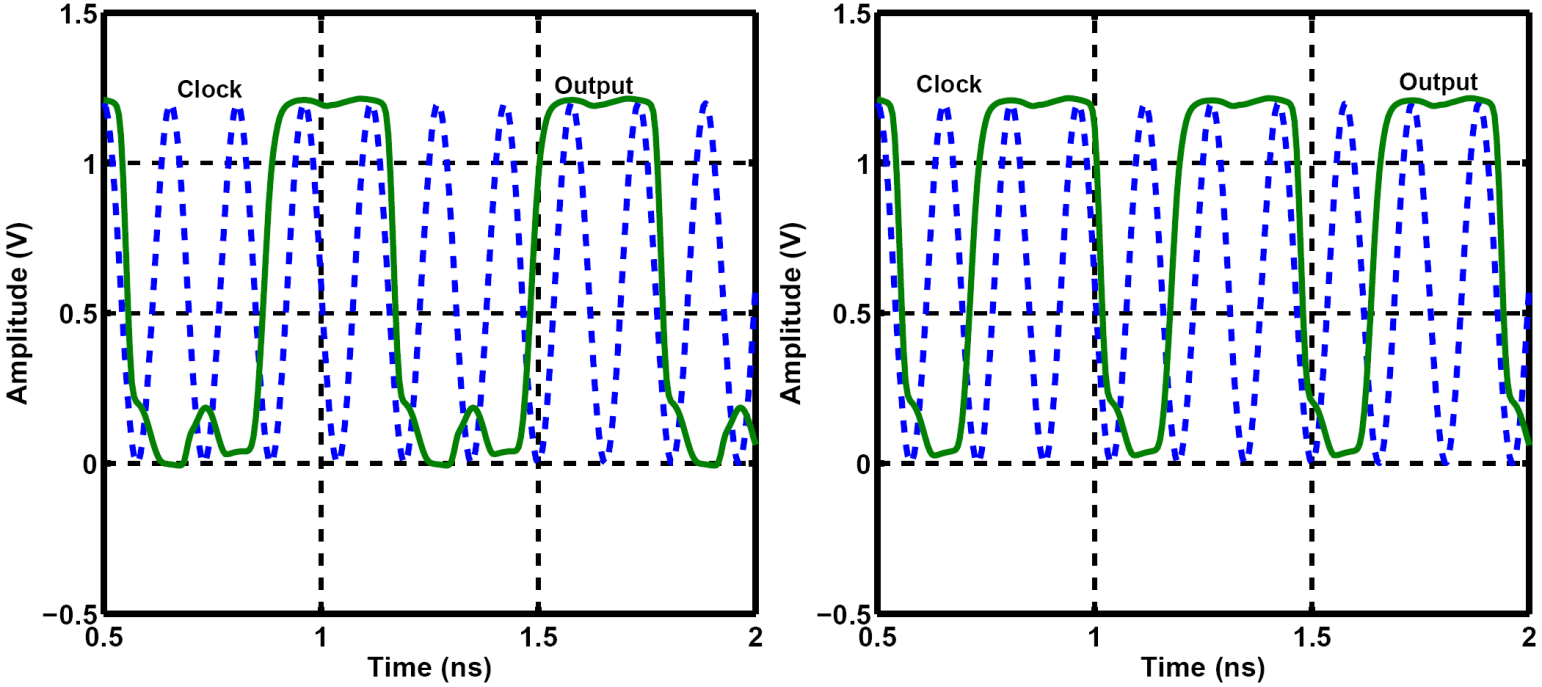
**We must now add an OR gate to the above topology to obtain a ÷ 3/4 circuit. Again, we prefer to merge this gate with either of the flipflops.**




- **The modulus control OR gate is embedded within the AND structure.**

# ÷3/4 Circuit: Simulation Result

**For a 6.5GHz clock, this ÷3/4 divider draws 0.5mA from a 1.2V supply.**




**For a frequency range of 5180 to 5320 in 20MHz steps, the division ratio of a presacler is NP+S=259 to 266. if S varies from 9 to 16, N=10 and P=25 and a ÷11/10 divider are needed. Or, N=5, P=50, a ÷5/6 divider are needed.**

**For high 11a carrier frequencies; 5745~5808MHz, a 5MHz reference is used. NP+S=1149- 1161. So, S=9~21, N=10 and P=114.**

# Loop Design

**The CP and LPF are designed based on the lowest value of *KVCO* ($2\pi$*200 MHz) and the highest value of the divide ratio, *M* (2x1161 for a 5MHz reference). We begin with a loop bandwidth of 500 kHz and a charge pump current of 1 mA. Thus, $2.5\omega_n = 2\pi$(500 kHz) and hence $\omega_n = 2\pi$(200 kHz). We have**

$$2\pi(200\,\text{kHz}) = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1 M}},$$

**If $I_p$ = 1 mA and $C_1$ = 54.5 pF, occupied a large area.**

**We instead choose $I_p$ = 2 mA and $C_1$ = 27 pF, trading area for power consumption. Setting the damping factor to unity,**

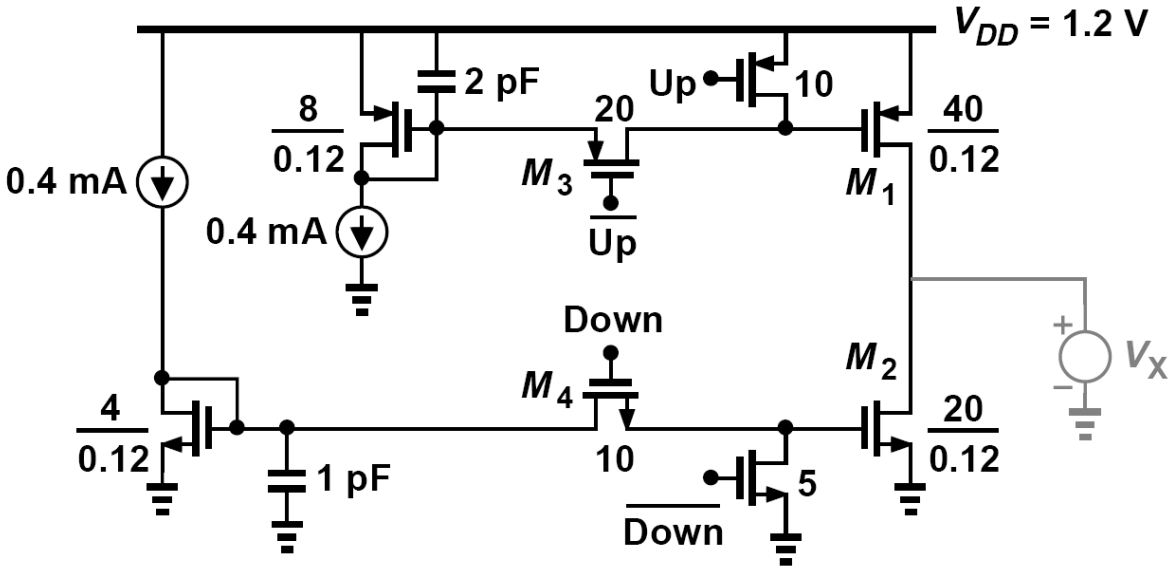
$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{VCO} C_1}{2\pi M}} = 1$$

**$R_1$ = 29.3k ohm and $C_2$ =$C_1$/5= 5.4 pF (section 9.7)**

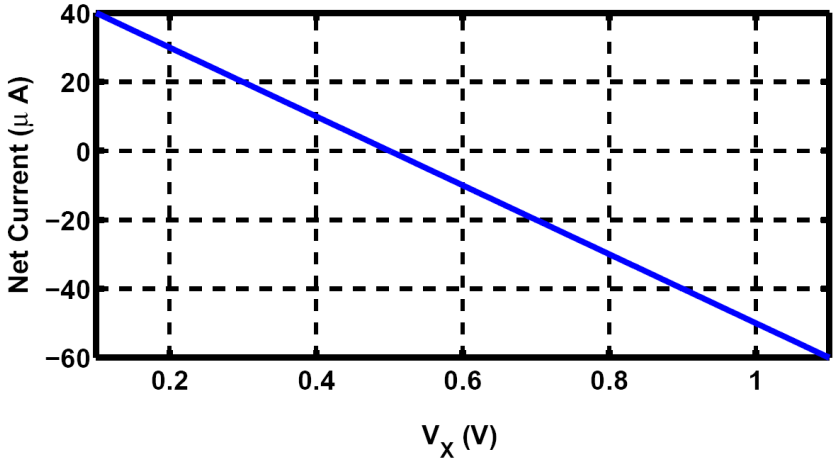
# Charge Pump

**For the charge pump, we return to the gate-switched topology as it affords the maximum voltage headroom.**

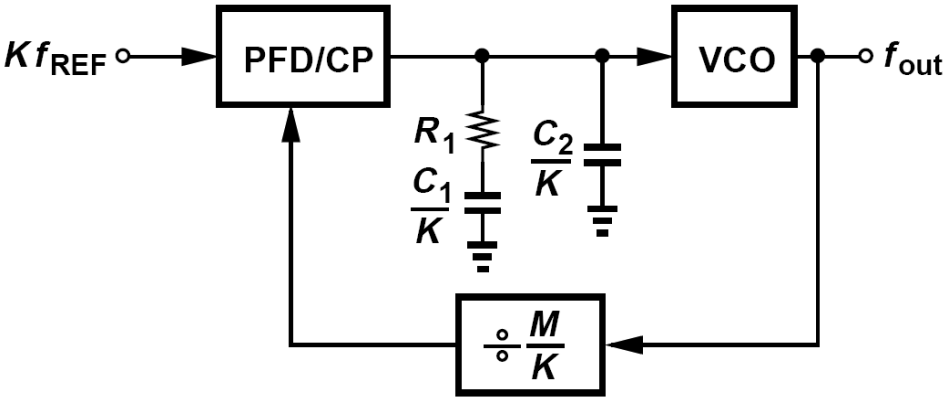
- **The gate-switched topology still proves rather slow, primarily because of the small overdrive of $M_3$ and $M_4$**

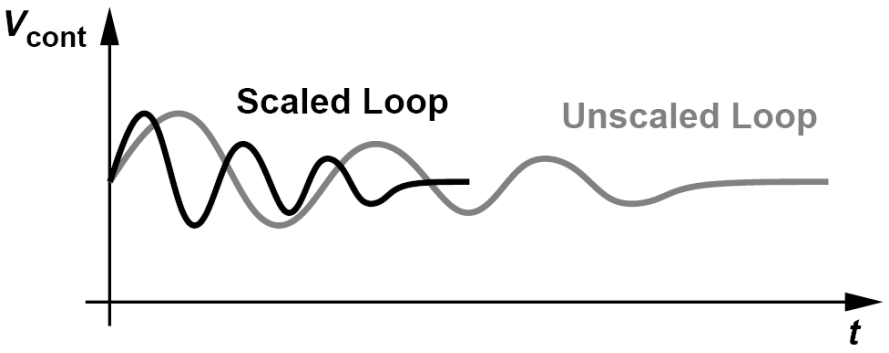



- **In this design, the maximum mismatch occurs at $V_{out}$ = 1.1 V and is equal to 60$\mu$A, about 3%.**



# Loop Simulation: Time Contraction

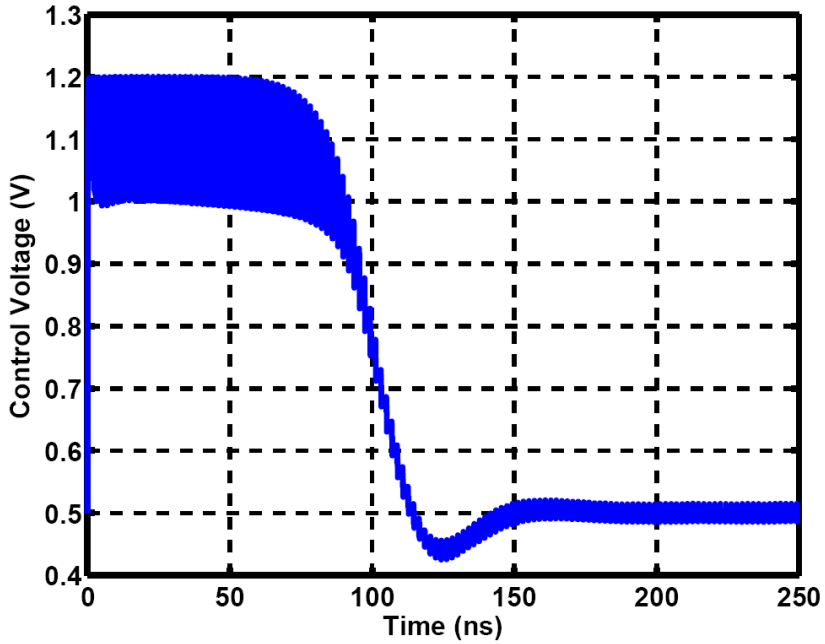


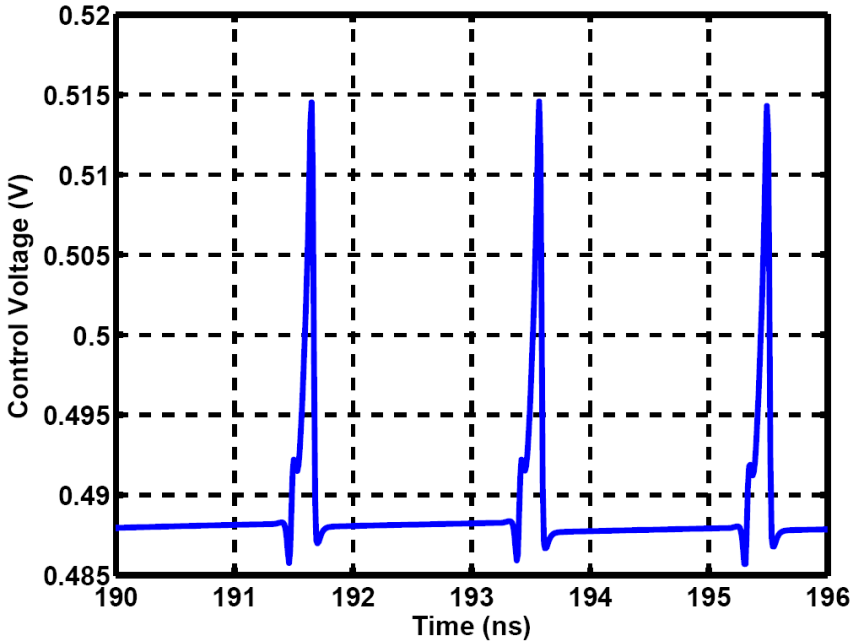




- We wish to scale down the lock time of the loop by a large factor, e.g., $K = 100$. To this end, we raise $f_{REF}$ by a factor of $K$ and reduce $C_1$, $C_2$, and $M$ by a factor of $K$.
- Note that time contraction does not scale $R_1$, $I_p$, or $K_{VCO}$, and it retains the value of $\zeta$ while scaling down the loop "time constant," $(\zeta\omega_n)^{-1} = 4\pi M/(R_1 I_p K_{VCO})$, by a factor of $K$.

# Loop Simulation: Behavioral Model

**In addition to time contraction, we also employ a behavioral model for the VCO with the same value of $K_{VCO}$ and $f_{out}$**



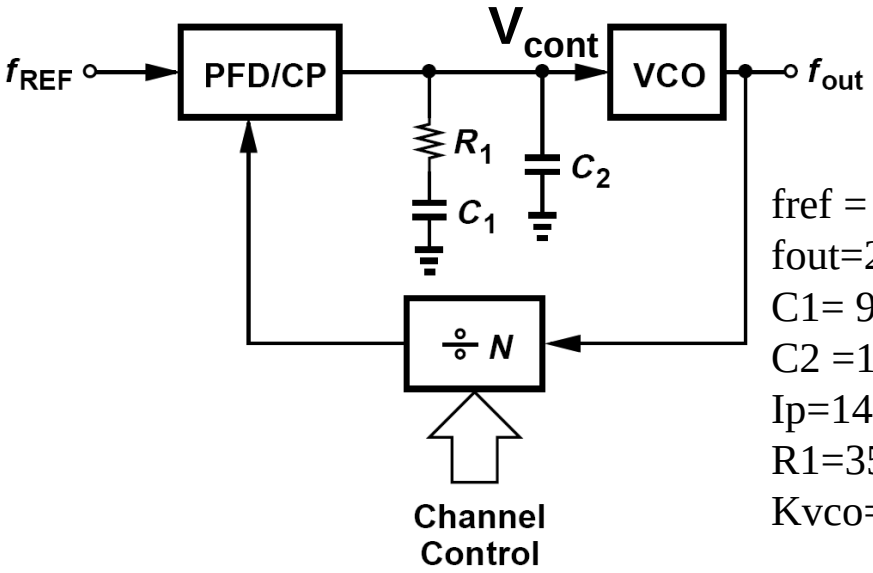




- **The PFD, the CP, and the loop filter incorporate actual devices, thus producing a realistic ripple. The loop locks in about 150 ns, incurring a peak-to-peak ripple of nearly 30 mV.**
- **We observe that our choice of the loop parameters has yielded a well-behaved lock response. This simulation takes about 40 seconds.**

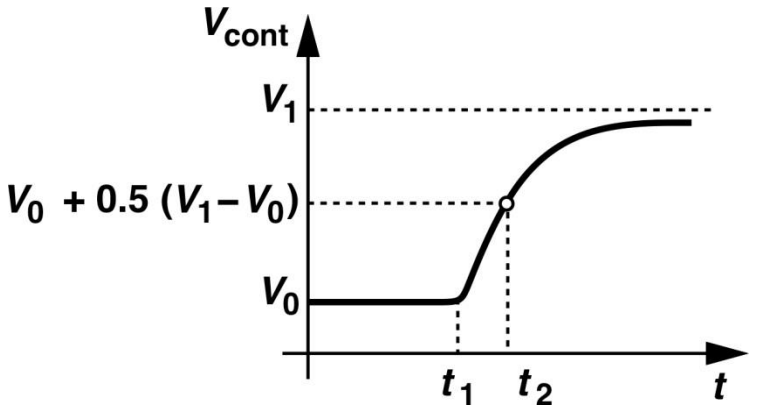
# Simulations of Transfer Function

- One-pole approximation

B. Razavi, Design of CMOS Phase-locked Loops, Ch 9.5, pp. 289




fref = 20 MHz
fout=2.4GHz
C1= 9.3 pF
C2 =1.86 pF
Ip=140 μA
R1=35.9kΩ
Kvco=400MHz/V




- Approximate the transfer function of a PLL as a one-pole system. The PLL locked at V0 & V1.
- t2-t1= τ x ln(2)=0.69x τ, where τ is the time constant.
- The closed-loop bandwidth is 1/(2πτ)
- Note as ζ=1, it leads to two conincident poles and the one pole approximation does not hold.

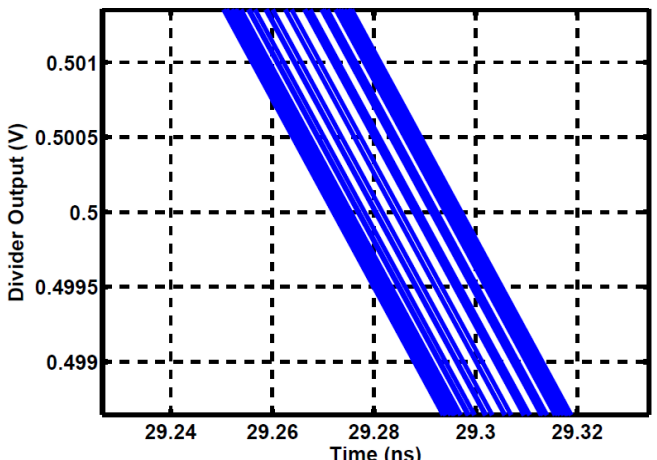
# Simulations of Transfer Function

- **By input FM source**

$$V_{FM}(t) = V_a + V_a \cos[\omega_{REF} t + K \int \cos \omega_m t dt]$$

$$V_{FM}(t) = V_a + V_a \cos\left(\omega_{REF} t + \frac{K}{\omega_m} \sin \omega_m t\right)$$

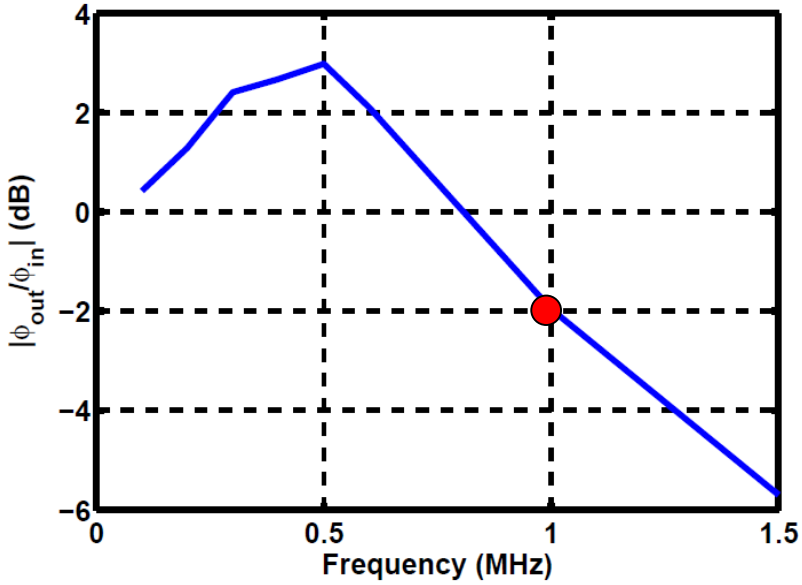
- **A clock with an input frequency is modulated by a cosine. Its input peak-to-peak phase variation is 2K/ωm and the output phase variation should be reduced by a factor of √2 at the -3dB frequency.**
- **While ωm= 2π(1MHz) with a peak-to-peak jitter of 31ps, the transient simulation is done ( simulation time is over 1us after the PLL locked). The simulated PLL at the divider output with a peak-to-peak jitter of 25ps.**
- **It translate to an attenuation of 1.9dB.**



# Simulations of Transfer Function

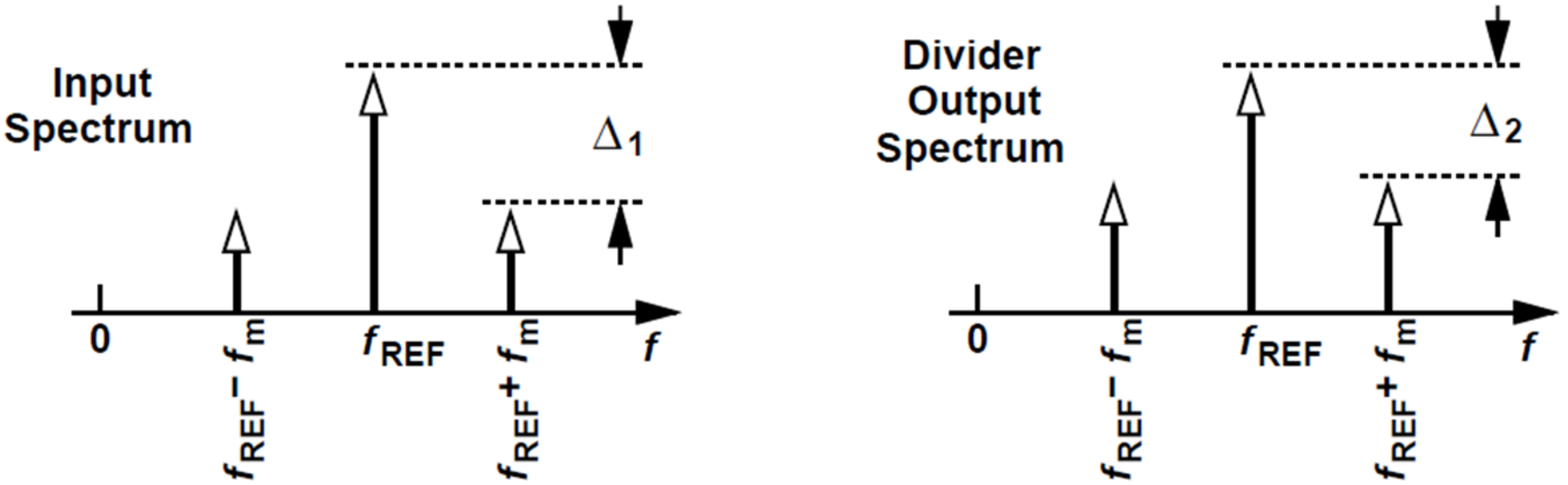
- **Do the transient simulations for various ωm.**
- **Estimated $\omega_{3dB}$ is around 1.2MHz.**

fref = 20 MHz
fout=2.4GHz
C1= 9.3 pF
C2 =1.86 pF
Ip=140 μA
R1=35.9kΩ
Kvco=400MHz/V




- **Calculated ωz= 1/(2π C1R1)~477kHz, $\omega_{3dB}$=2π (2.4MHz)**
- **It is not consistent between the calculations and simulations. It is partially occurs because the pole caused by C2R1 is not far from the unity gain frequency.**

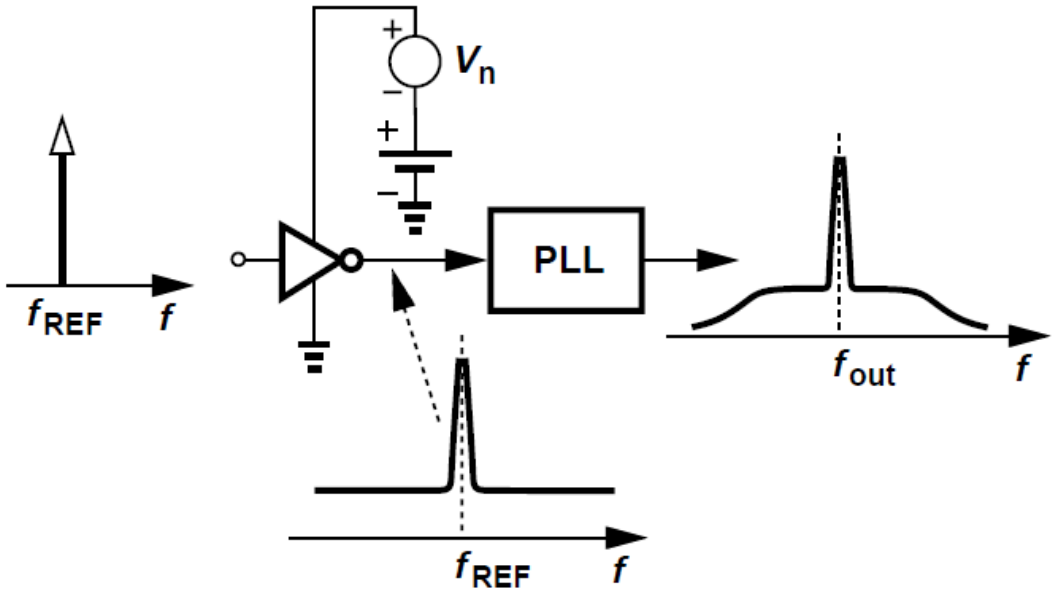
# Simulation/Measurement of Transfer Function




- **By observing both input and output spectra, the sidebands are induced by phase modulations.**
- **The ratio of input to output jitter is given by Δ2+20Log(N) - Δ1 in dB (N is the divide ratio of 120).**
- **Note that the measurement can be done by this way.**

IEEE TCAS-II, vol. 68, pp. 873-, March 2021.

# Simulations of Phase Noise & Transfer Function

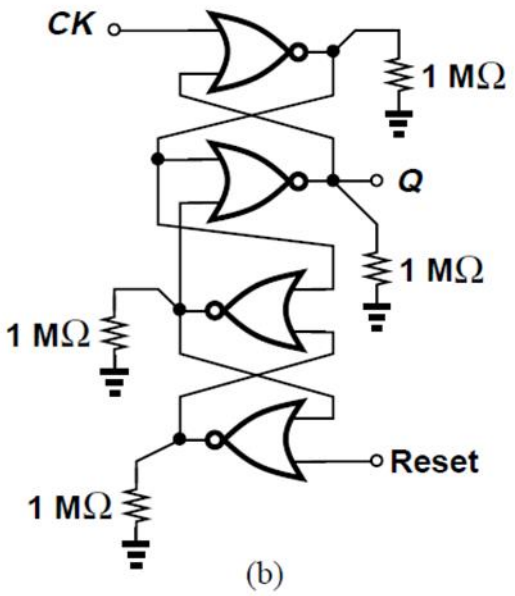



- **A White-Noise-Spectrum voltage source is applied in series to the supply of the input inverter of the PLL.**
- **This noise modulates the delay of inverter thereby inducing an output phase that has a $K_{DD}$ different from $K_{VCO}$.**

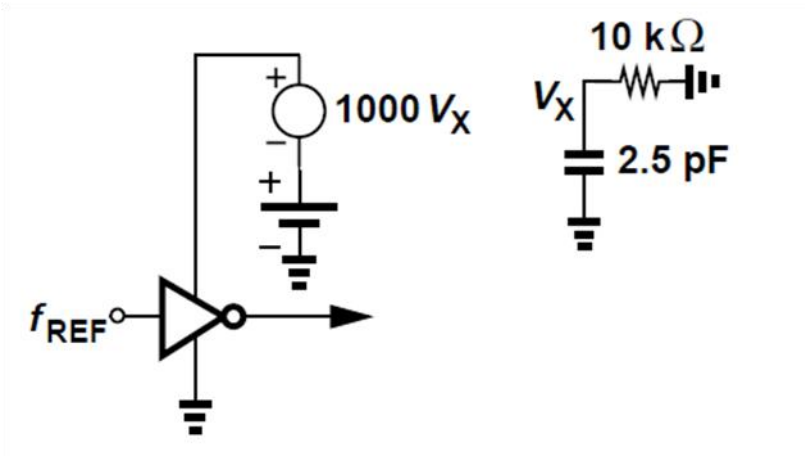
$$V_{inv}(t) = V_a + V_a \cos(\omega_{REF} t + K_{DD} V_n)$$

- **PSS (periodic steady state) and Pnoise (periodic noise ) analysis are done in Cadence to simulate the transfer function for the phase modulated input.**

# Simulations of Phase Noise & Transfer Function

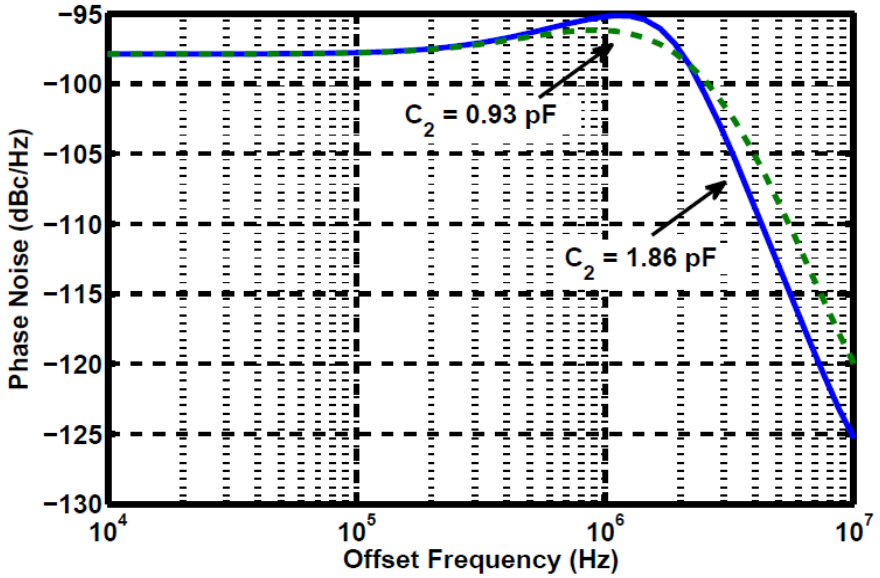


(b)




- To avoid the convergence issue, we put resistors of 1MΩ tied to ground for the NOR gates in pss simulation. The simulation time should be long enough such that the PLL settles.
- RC network is used to generate a band-limited noise which is amplified 1000 times so that this phase modulation far exceeds the intrinsic PLL phase noise.

# Simulations of Transfer Function




- Since the PLL's internal noise sources contribute much less phase noise, the phase noise plots reflect the PLL transfer function.
- For C2=1.86pF, the noise peak is 2.7dB and ω3dB=2π (2.5MHz) which close to the calculated 2.4MHz.
- For C2=0.93pF, the noise peak is 1.7dB and ω3dB=2π (2.8MHz)
- A lower C yields lower area under phase noise plot (random jitter reduces) but the ripple in Vcont increase (deterministic jitter increases)